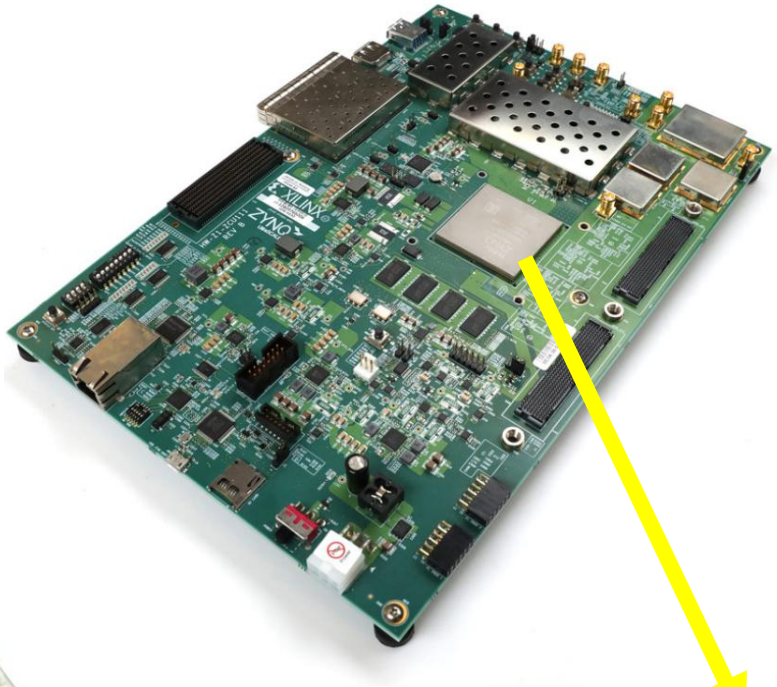
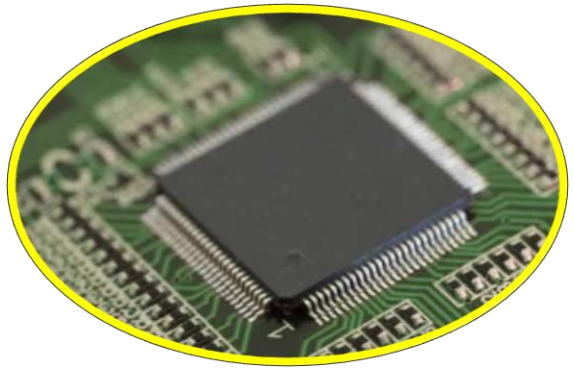

MATLAB
EXPO
POLSKA 2024

FPGA

Common part!





Oprogramowanie Naukowo-Techniczne sp. z o.o.

MATLAB EXPO

Warszawa, 4.06.2024 r.

FPGA-based hardware support from MATLAB

Features and workflows

Mateusz Łabęcki, ONT

MathWorks Authorized Reseller

From MATLAB Algorithm to HDL Implementation

```
TxSignal = zeros(TxLen,1);
TxSignal(PulseLoc:PulseLoc+PulseLen-1) = pulse;

% Create Rx signal by adding noise
Noise = complex(randn(TxLen,1),randn(TxLen,1));
RxSignal = TxSignal + Noise;

% Scale Rx signal to +/- one
scale1 = max([abs(real(RxSignal)); abs(imag(RxSignal))]);
RxSignal = RxSignal/scale1;

%% MATLAB golden reference

% Create matched filter coefficients
CorrFilter = conj(flip(pulse))/PulseLen;

% Correlate Rx signal against matched filter
FilterOut = filter(CorrFilter,1,RxSignal);

% Find peak magnitude & location
[peak, location] = max(abs(FilterOut));
```

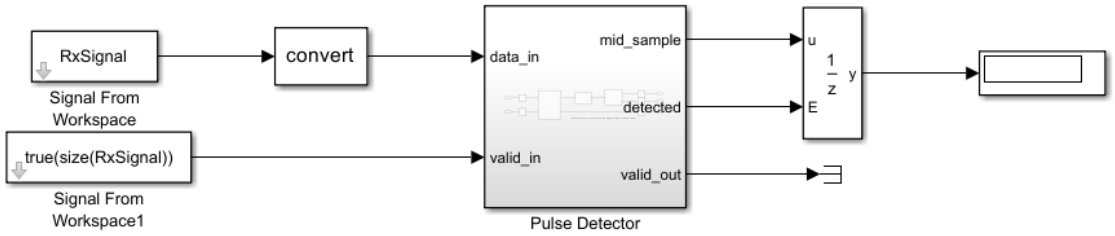
HDL Code generation

HDL Code

symmetric_fir.vhd (10) Search

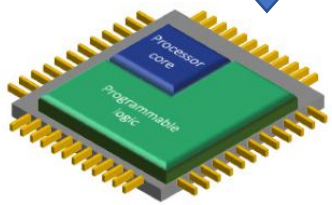
ud3 1 / 10

```
123
124  ud2_process : PROCESS (clk, reset)
125  BEGIN
126    IF reset = '1' THEN
127      ud2_out1 <= to_signed(16#0000#, 16);
128    ELSIF clk'EVENT AND clk = '1' THEN
129      IF enb = '1' THEN
130        ud2_out1 <= ud1_out1;
131      END IF;
132    END IF;
133  END PROCESS ud2_process;
134
135
136  ud3_process : PROCESS (clk, reset)
137  BEGIN
138    IF reset = '1' THEN
139      ud3_out1 <= to_signed(16#0000#, 16);
140    ELSIF clk'EVENT AND clk = '1' THEN
141      IF enb = '1' THEN
142        ud3_out1 <= ud2_out1;
143      END IF;
144    END IF;
145  END PROCESS ud3_process;
146
```



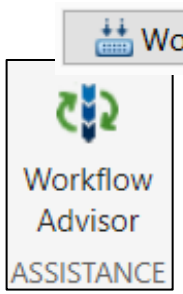
Synthesizable RTL Code

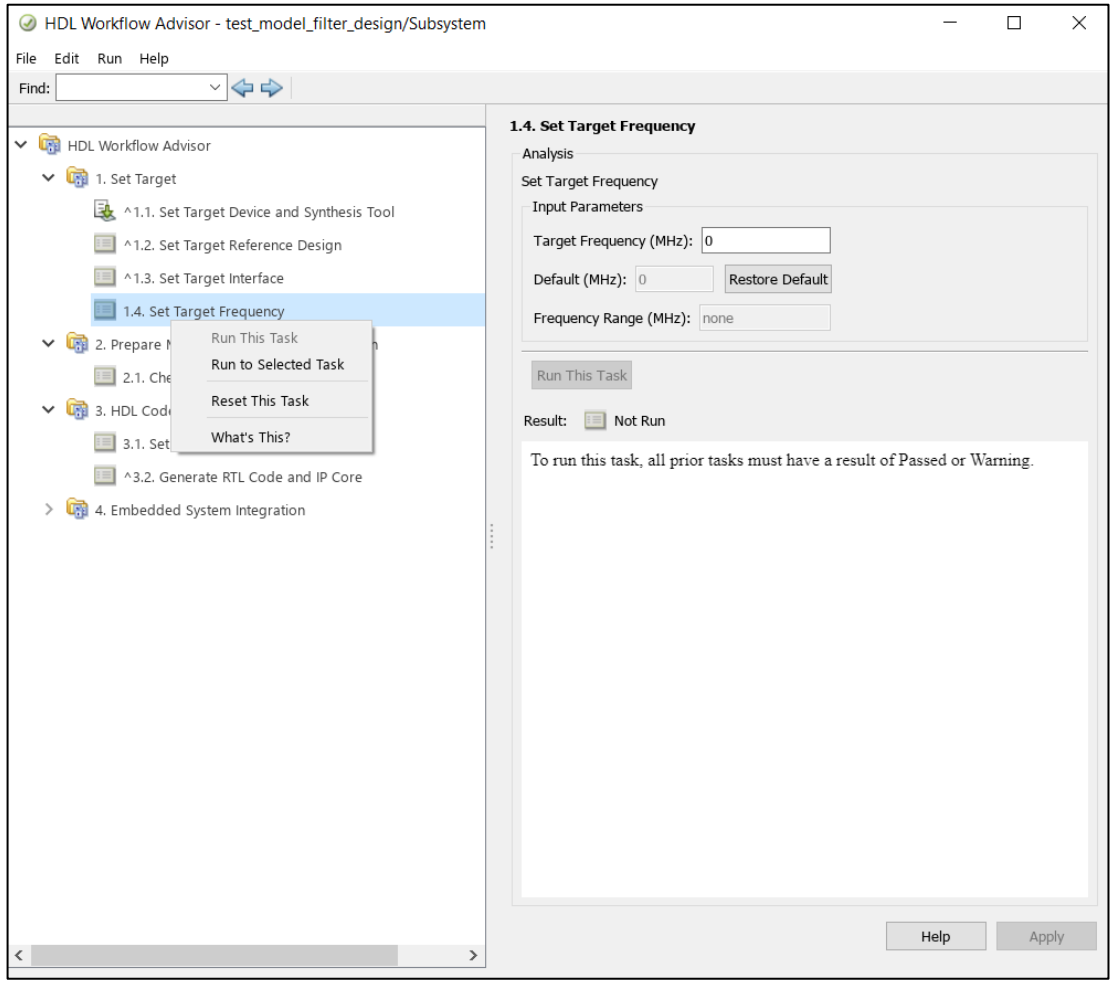
Synthesis & Implementation

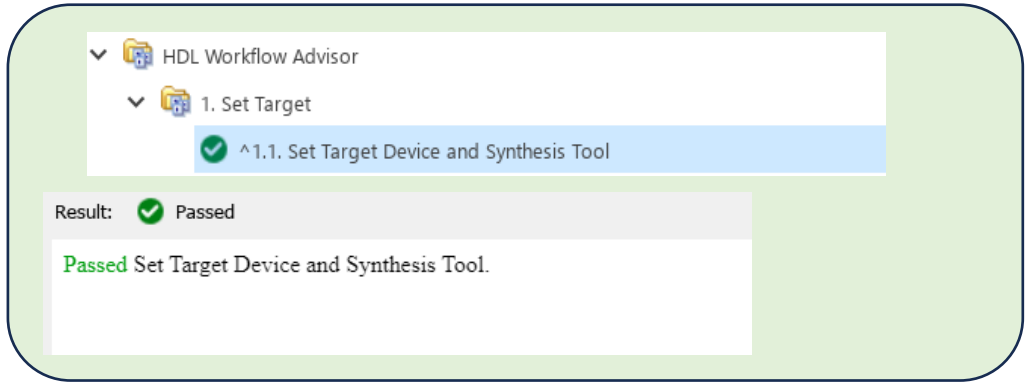


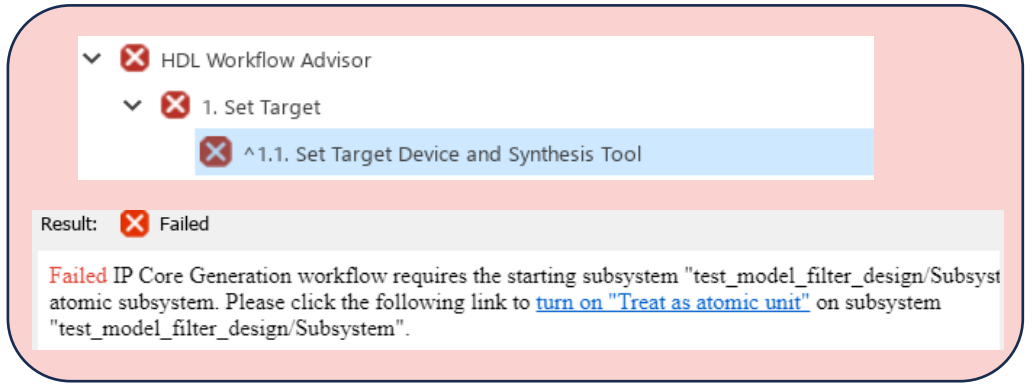
Standalone FPGA

Code Generation with HDL Workflow Advisor



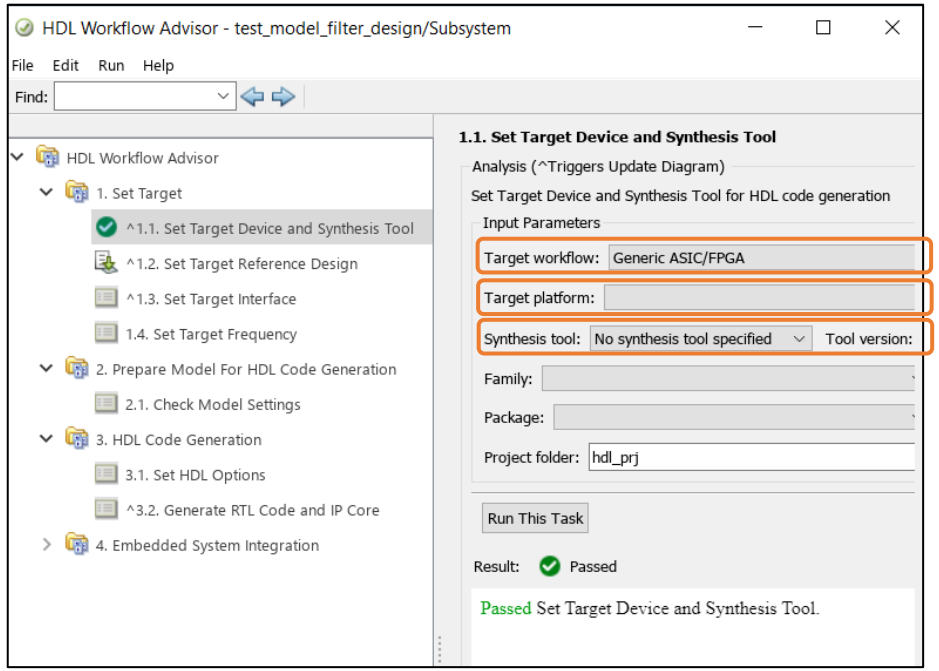


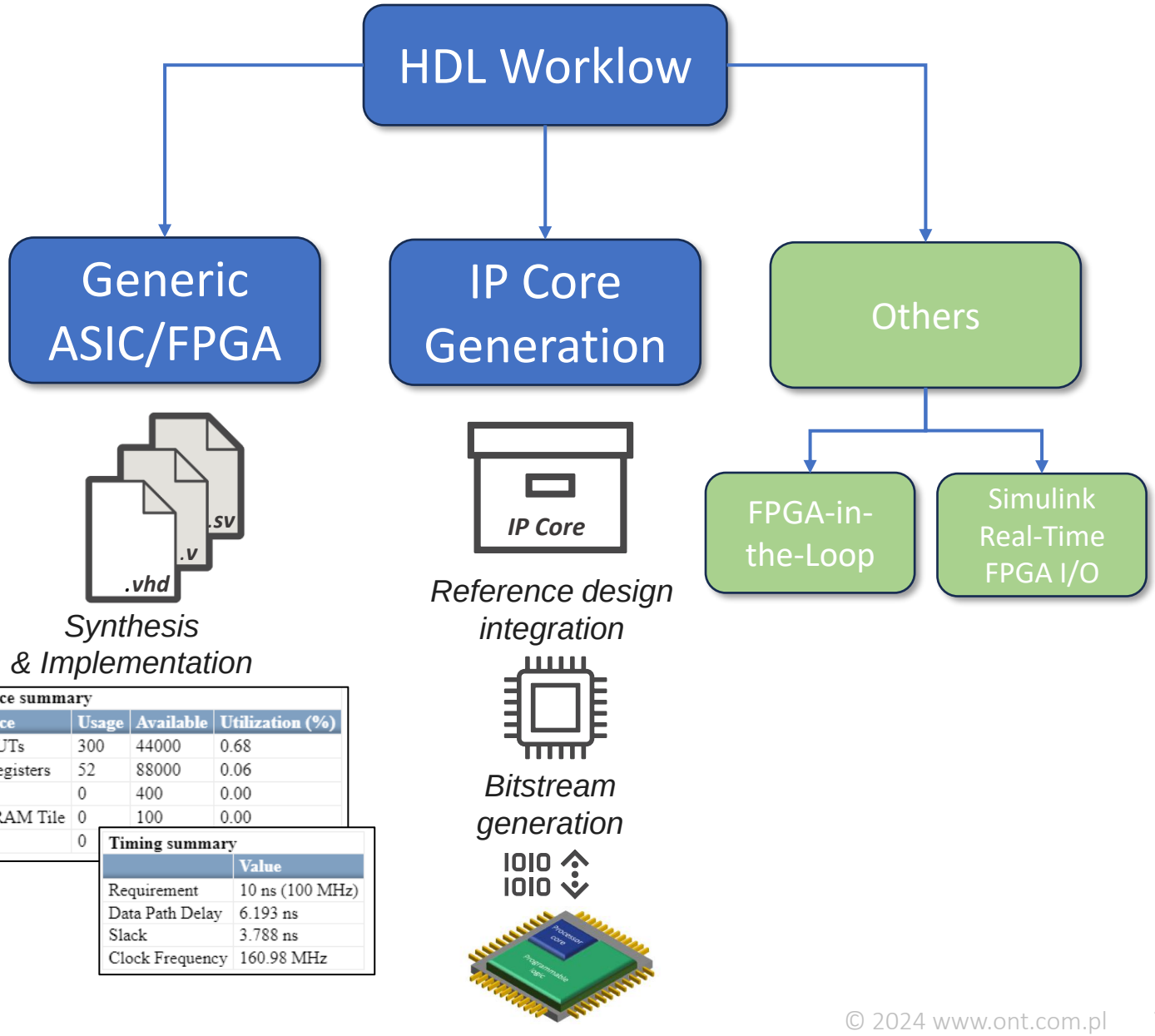




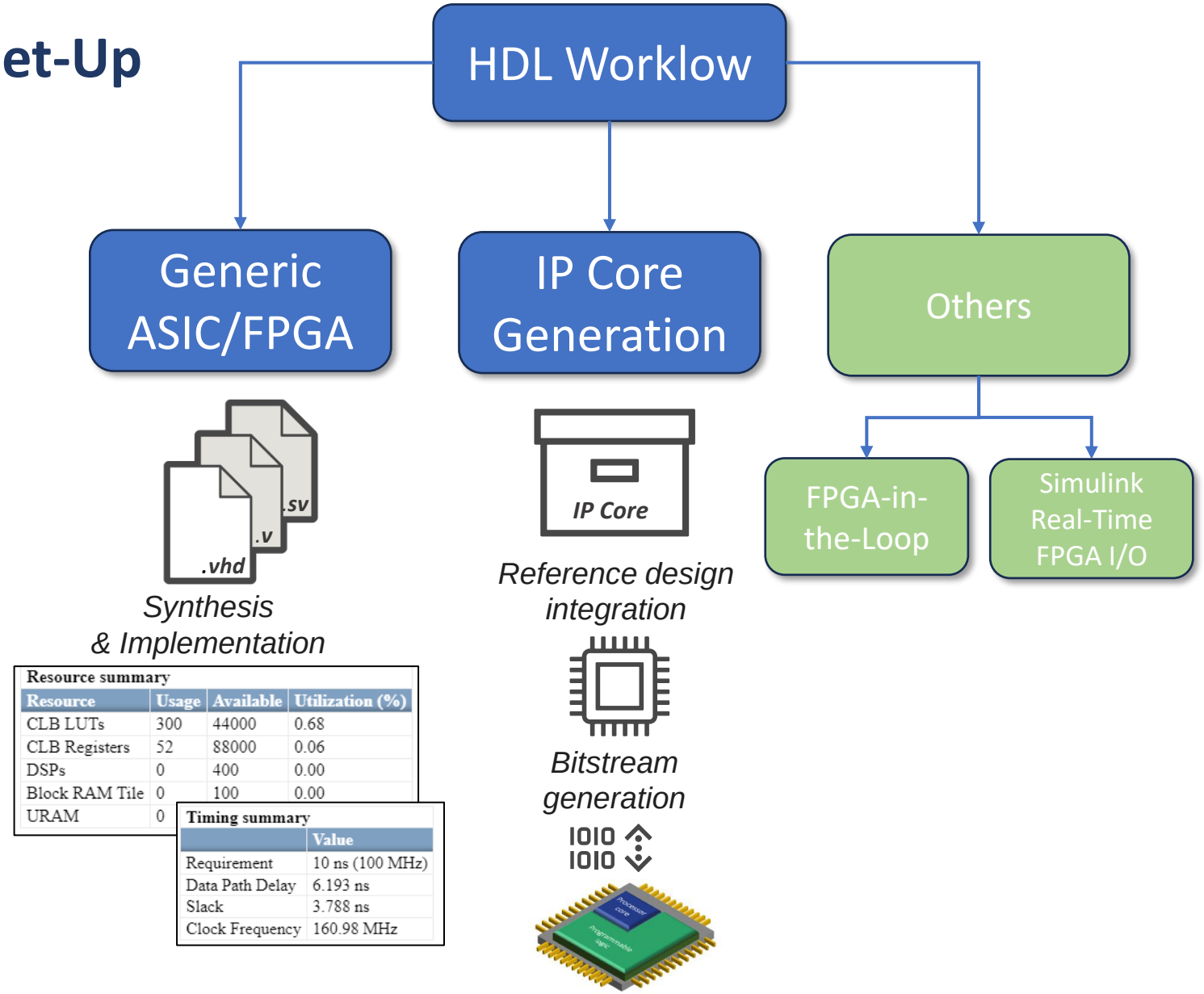
HDL Workflow Set-Up

- Settings that affect Advisor's steps:
  - **a) Target workflow**
  - **b) Target platform**
  - **c) Synthesis tool**





HDL Workflow Set-Up



System-on-Chip

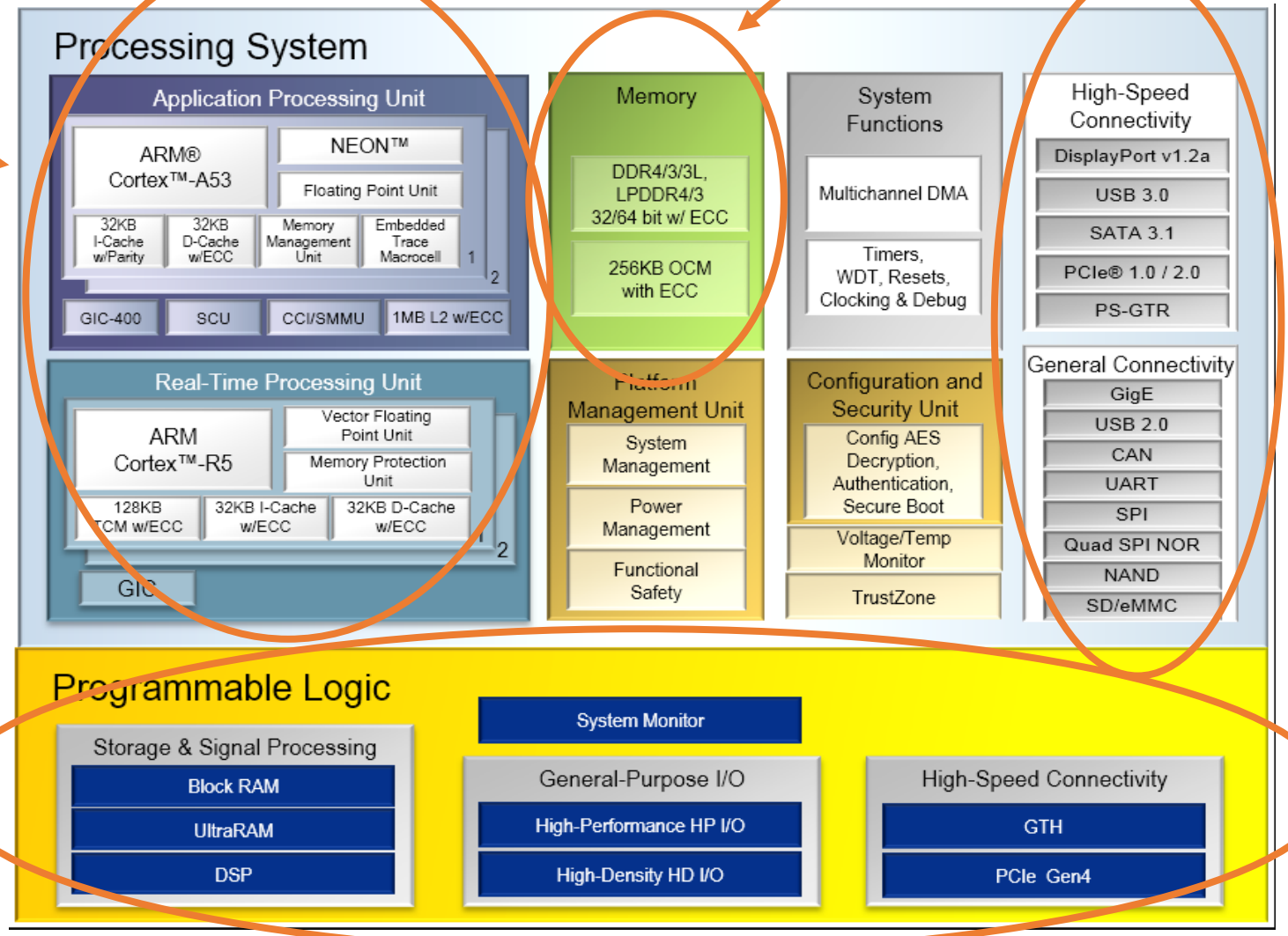
Targeting SoC

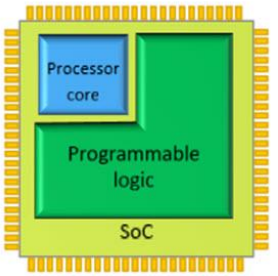
Multiple Processors

Memory Interfaces

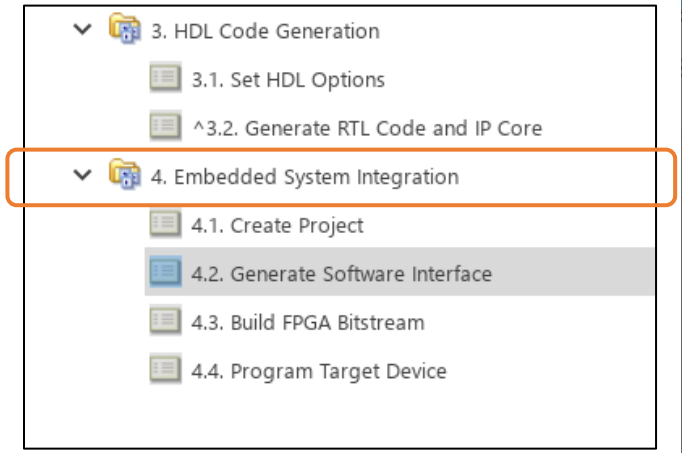
Programmable FPGA Logic

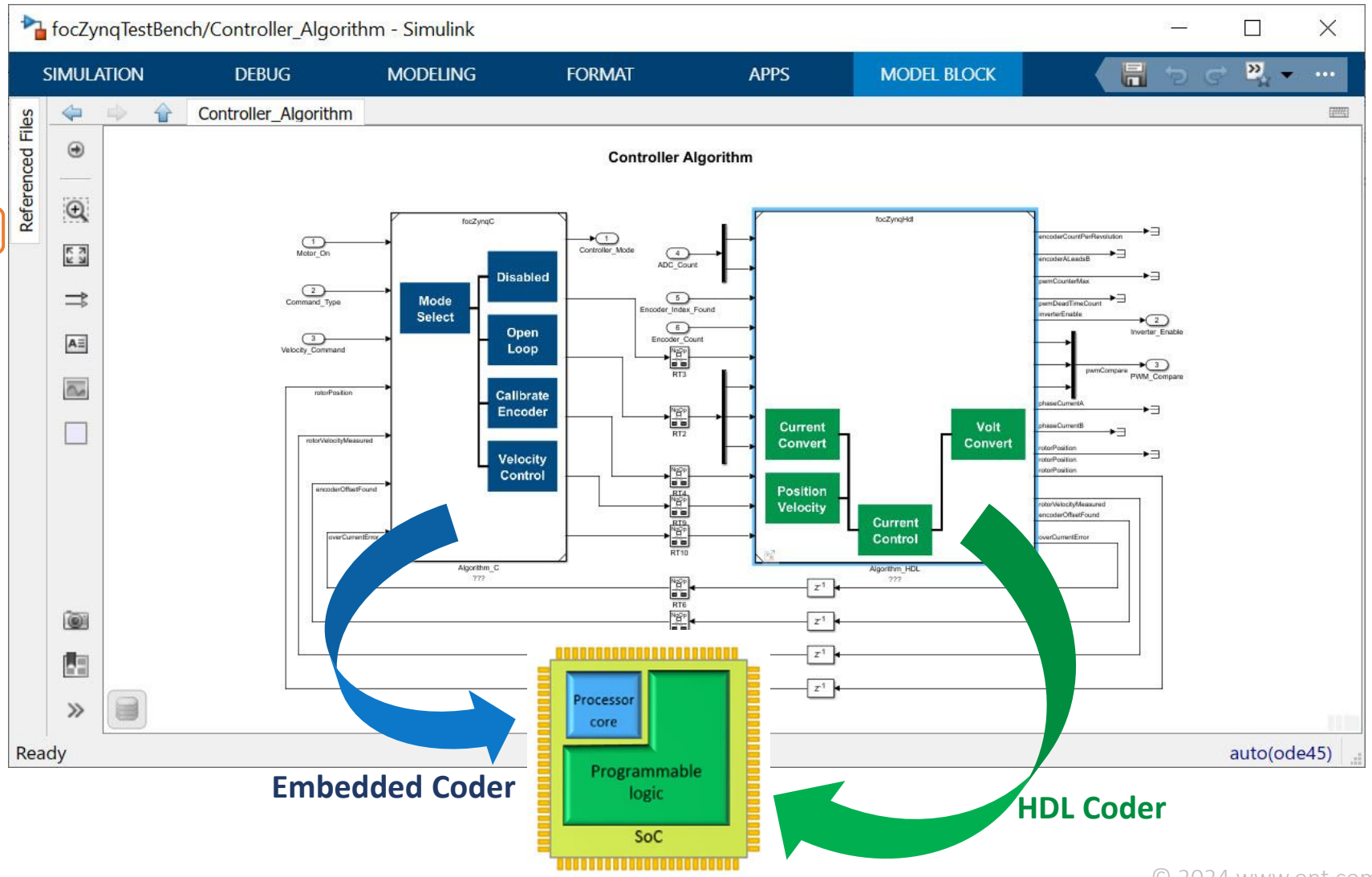
Communication Interfaces



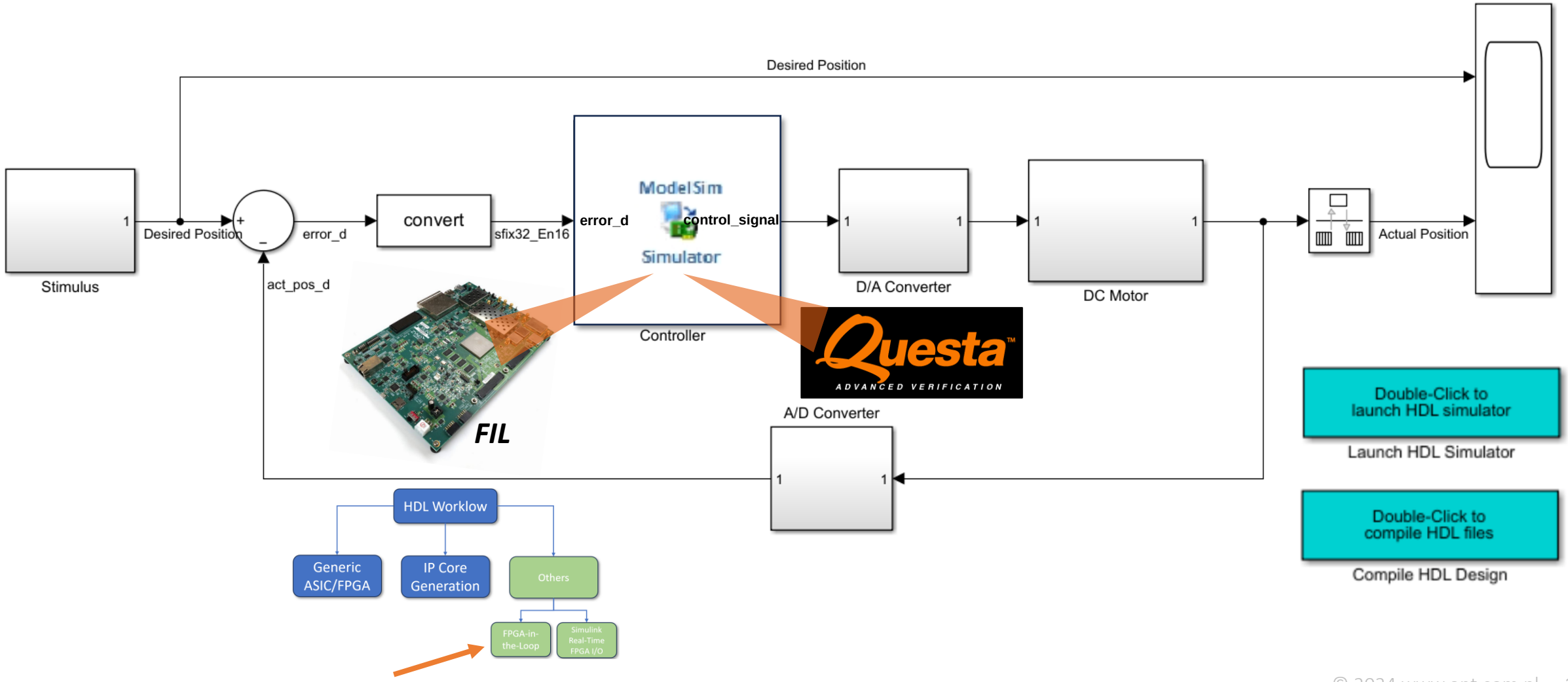


Hardware-Software Partition



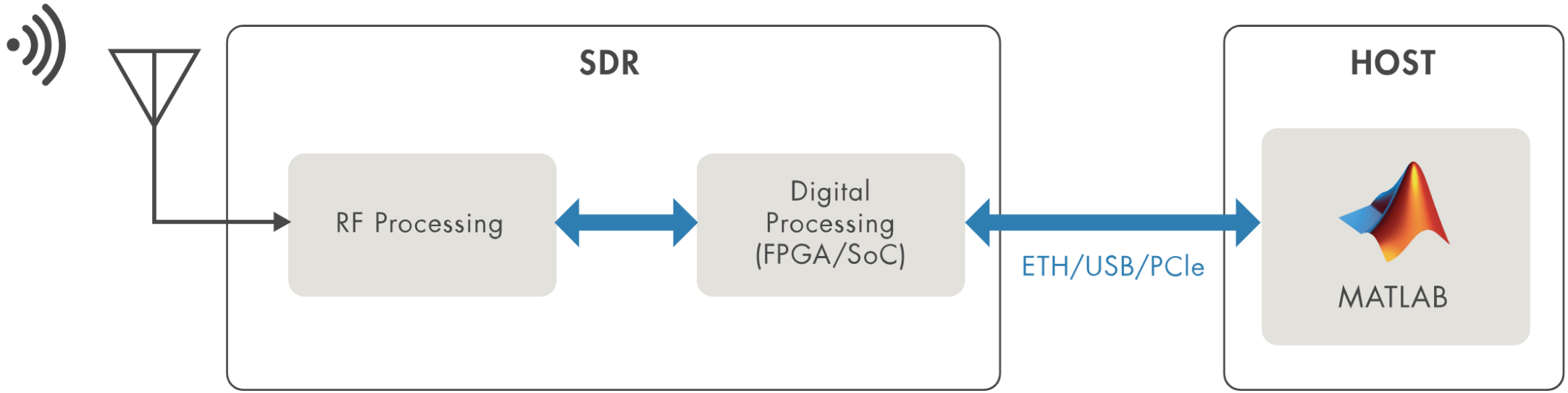


Next steps in MATLAB/Simulink – HDL Verification



Software-Defined Radio

Support from Communications Toolbox



ADALM-PLUTO Radio Support from Communications Toolbox

Prototype a Devices AD

USRP E310 Support from Communications Toolbox

Prototype and E310 with MA

USRP Support from Communications Toolbox

Design and pr USRP with MA

RTL-SDR Support from Communications Toolbox

Design and prototype software-defined radio (SDR) systems using RTL-SDR with MATLAB and Simulink

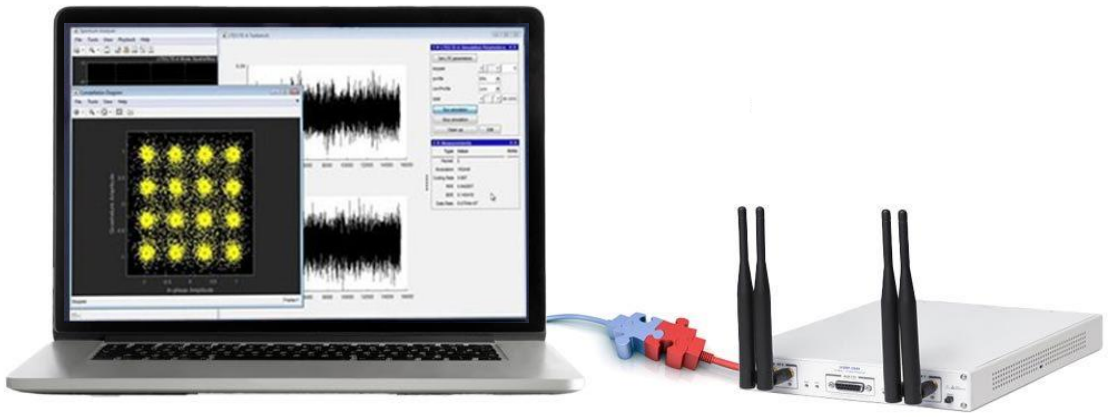
Pluto Receiver	Receive data from Analog Devices ADALM-PLUTO radio
Pluto Transmitter	Transmit data to Analog Devices ADALM-PLUTO radio
RTL-SDR Receiver	Receive data from RTL-SDR device
E3xx Receiver	Receive data from USRP E3xx radio hardware *(Since R2019b)*
E3xx Transmitter	Send data to USRP E3xx radio hardware *(Since R2019b)*
SDRu Receiver	Receive data from USRP device
SDRu Transmitter	Send data to USRP device

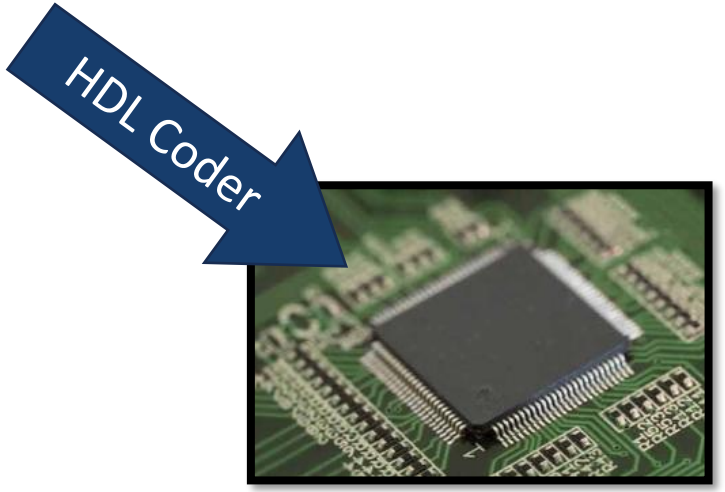
Support for high-end USRPs from Wireless Testbench

- Supported USRP Radios:
  - **X4xx**
  - **X3xx**
  - **N3xx**

Ettus Research™
A National Instruments Company

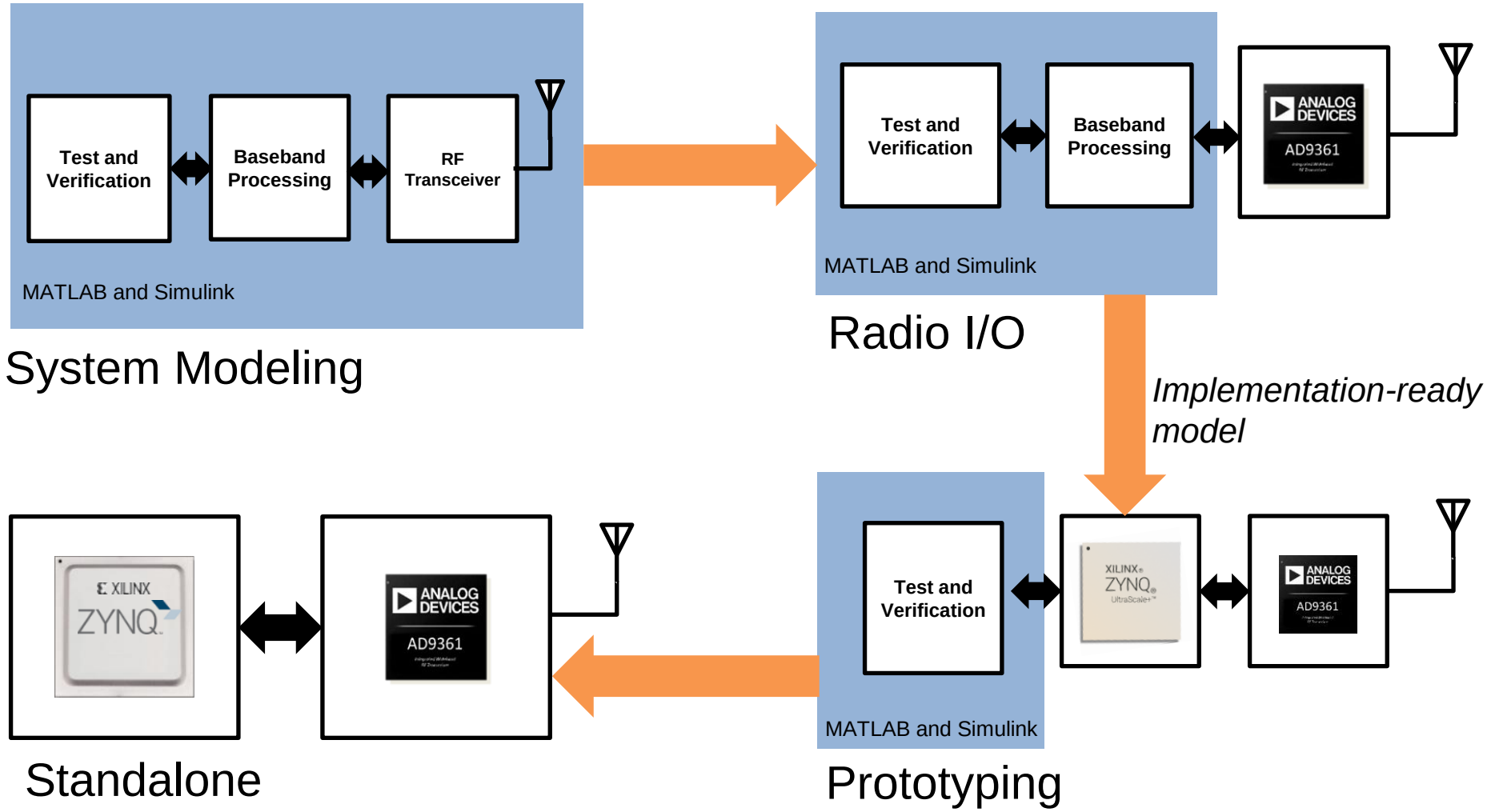
- Common Applications:
  - Transmit and capture standard-based and custom wideband signals
  - Intelligent signal detection using preamble and energy level
  - Run prebuilt and custom wireless applications on the FPGA/SoC on USRP hardware



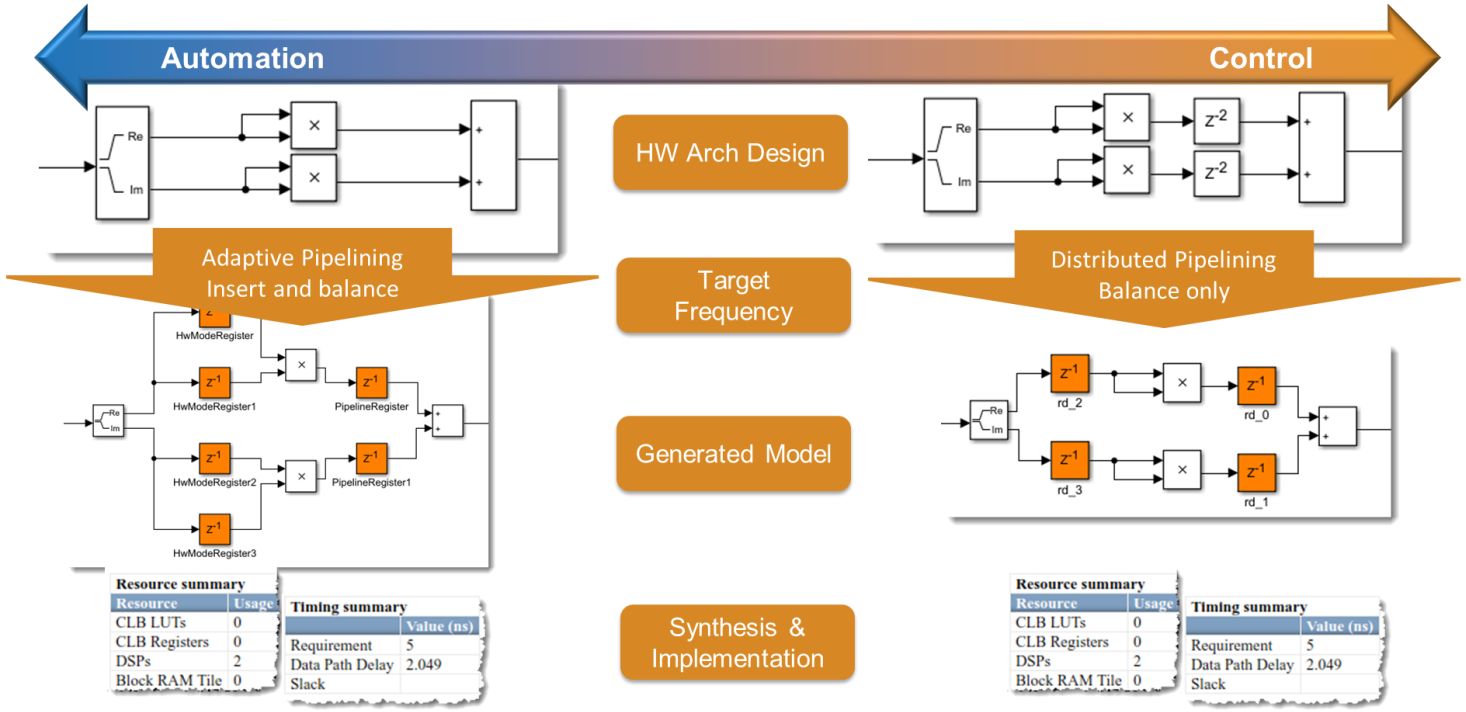


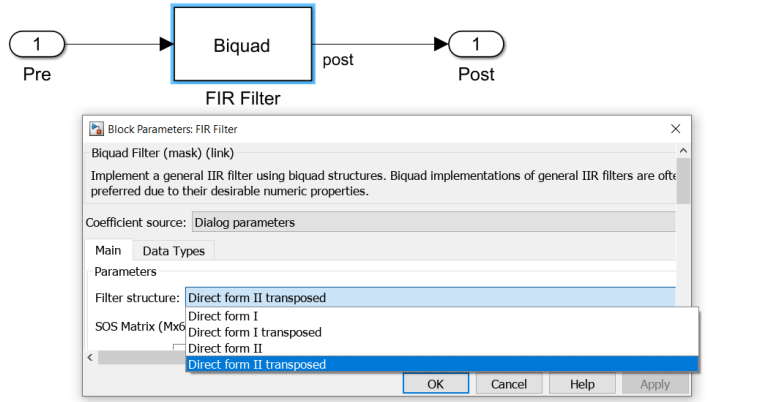
USRP FPGA Targeting

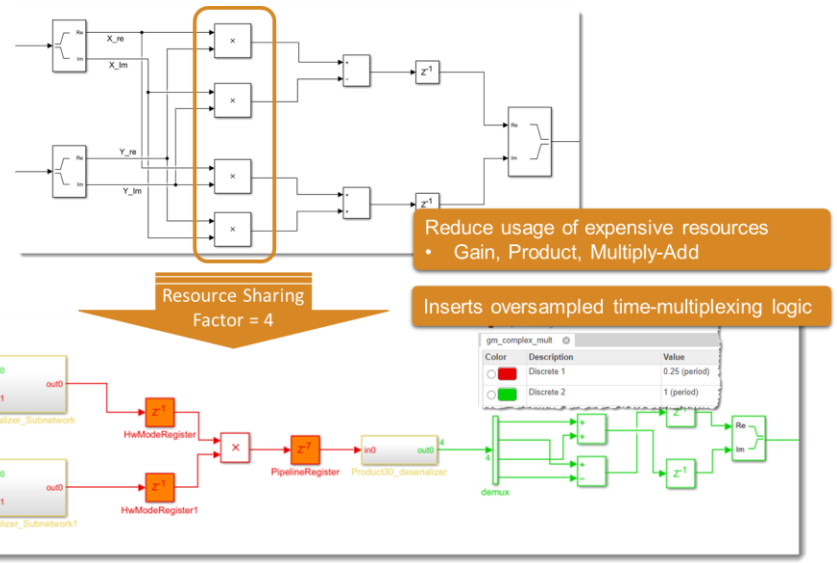
SDR Design Workflows



Further Exploration - Optimization







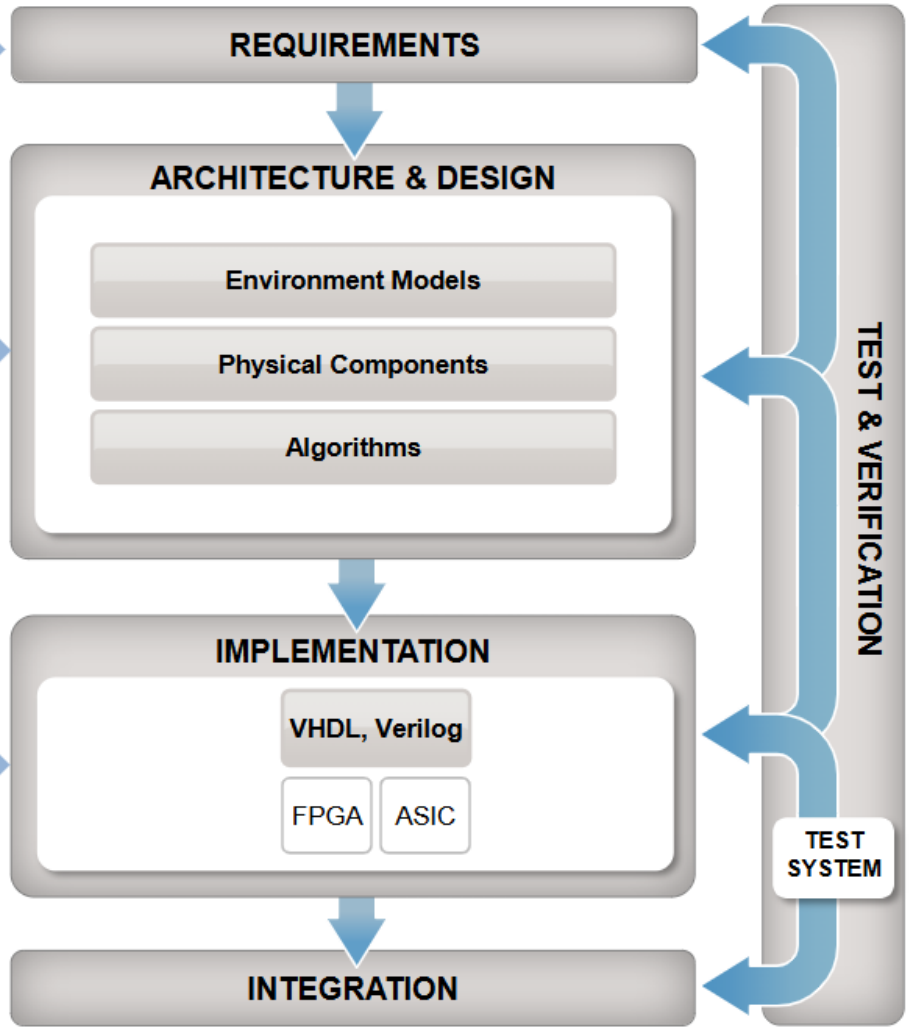
- Timing optimization – pipelining
- Area optimization – resource sharing
- Both - Filter design optimization

Model-Based Design for FPGA

- Requirements Toolbox

- System Composer
- Simulink
- Stateflow
- MATLAB

- HDL Coder



- Simulink Check
- Simulink Test
- Simulink Coverage
- Simulink Design Verifier
- Simulink Report Generator

- HDL Verifier

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