Symulacja obwodowa modelu o zredukowanym rzędzie ROM (ANSYS Q3D) w środowisku MATLAB_Simulink

Rockwell Automation

expanding human possibility®

Agenda

1 About us and Rockwell Automation

2 Problem description

3 Equivalent DC link capacitor model

4 RLCG model of laminated busbars

ANSYS simulation

5 Multi-physics circuit simulations MATLAB/Simulink

6 ROM Model validation

7 DC/AC inverter simulations with busbar ROM model

8 Summary & future research

1. About us and Rockwell Automation

Rockwell Automation

Rockwell Automation – company introduction

Dr inż. Wojciech Jurczak

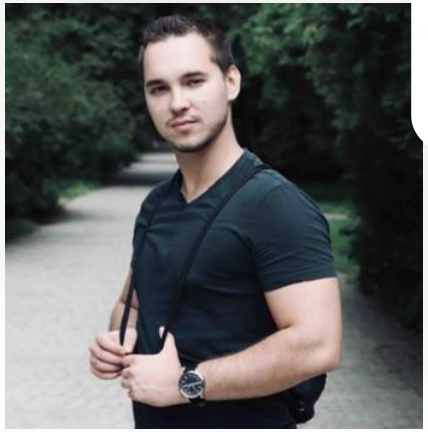
Power electronics architect

Low voltage drives

Mgr inż. Dawid Stawiarski

Power electronics engineer

Low voltage drives



Mgr inż. Kamil Zygmunt

Simulation engineer

Low voltage drives

expanding **human possibility**®

2800+ employes in Poland

PUBLIC

AT A GLANCE

Rockwell Automation

Our strategy is to bring The Connected Enterprise to life.

We integrate control and information across the enterprise to help industrial companies and their people be more productive and sustainable.

$9.1B
FISCAL 2023 SALES

29,000
EMPLOYEES

100+
COUNTRIES

ABOVE-MARKET GROWTH | PRODUCTIVITY | INTELLECTUAL CAPITAL >>> VALUE CREATION

1. About us and Rockwell Automation

PowerFlex®

Low Voltage Drives	Medium Voltage Drives	Programming & communication

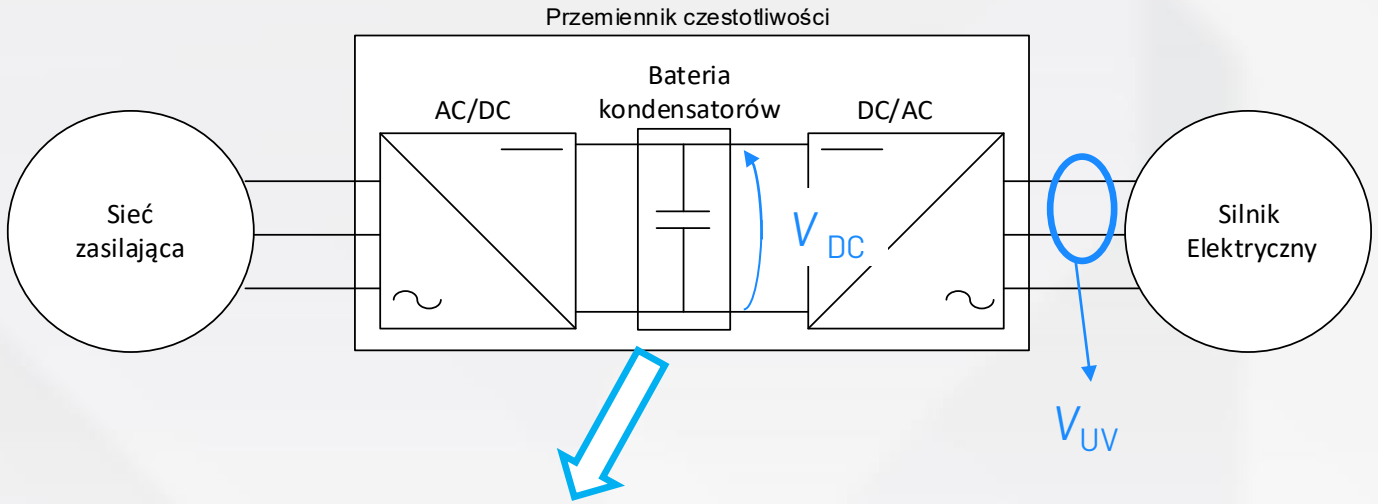
PowerFlex 755TS & 755TM
UL/IEC: 400/690 up to 4000A

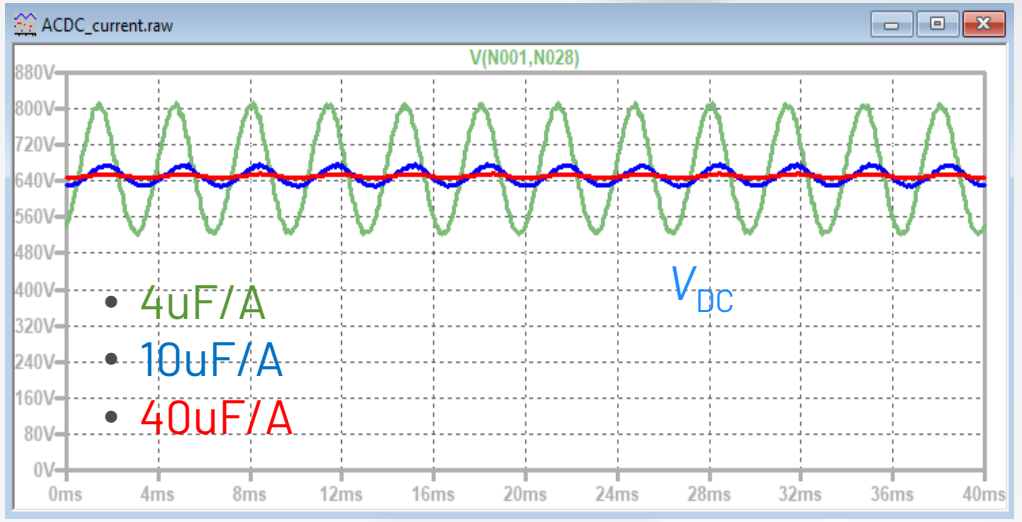
PowerFlex 6000 & 7000
UL/IEC: 2.3kV - 11kV up to 680A
UL/IEC: 2.3kV - 6.6kV up to 720A

DeviceNet
ControlNet
ProfiNet
ProfiBus

Rockwell Automation

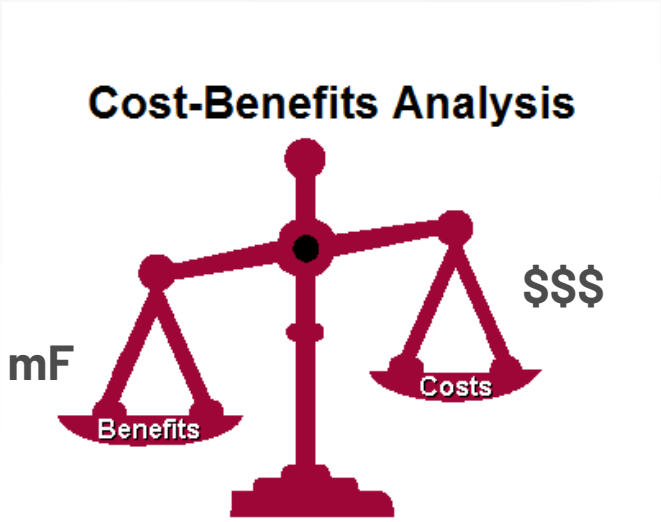
2. Problem description





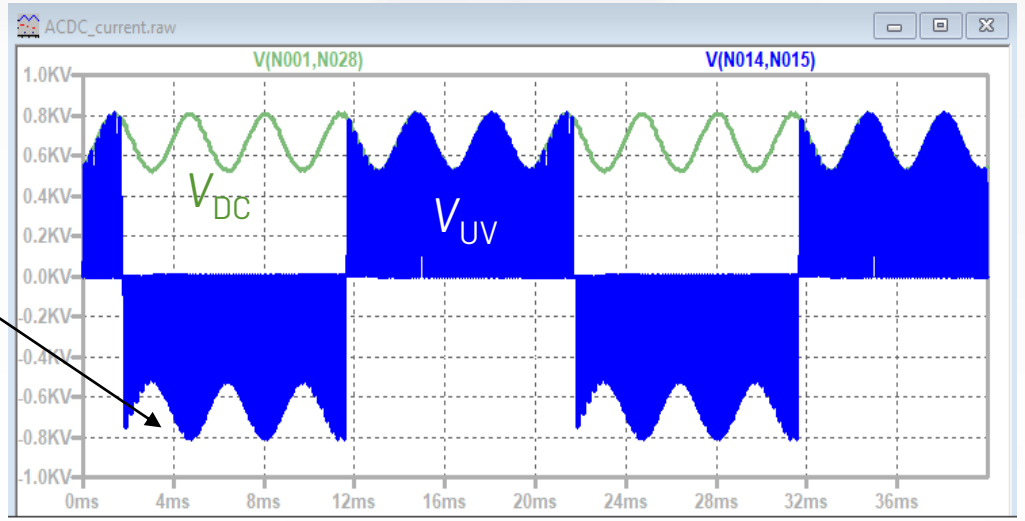
DC capacitor bank requirements

- **Capacitance vs V_{DC} ripples**

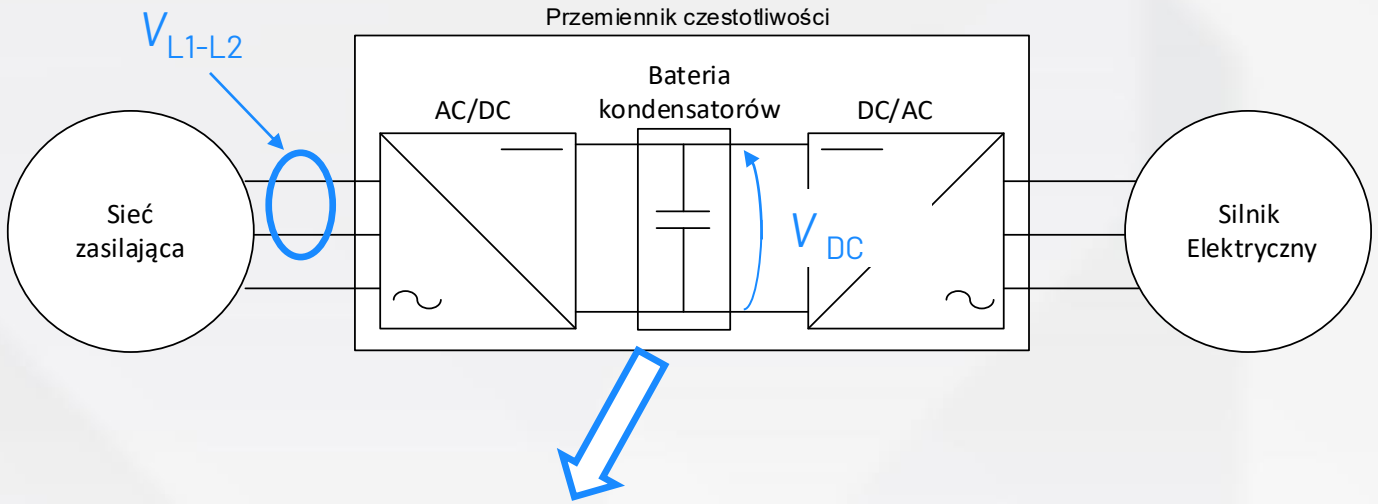


1. High V_{DC} ripples
2. Output voltage ripples
3. Motor torque ripples

- 4uF/A



2. Problem description



For 400/480 V_{AC} drives

- 564/677 V_{DC} Normal operation
- Up to 800V during motor deceleration

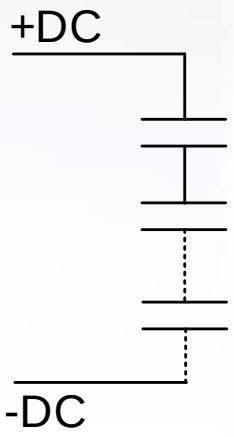
For 600/690 V_{AC} drives

- 846/973 V_{DC} Normal operation
- Up to 1100V during motor deceleration

$$V_{DC} = \sqrt{2} \cdot V_{L1-L2}$$

DC capacitor bank requirements

- Capacitance vs V_{DC} ripples
- **High DC voltage operation**



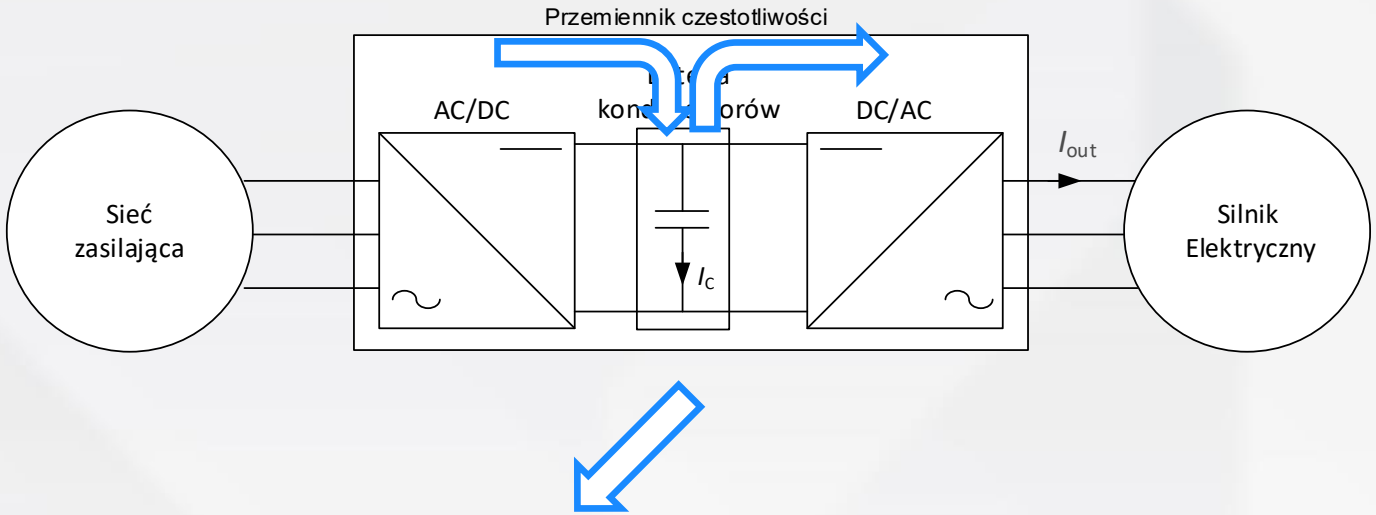
Series connetion needed

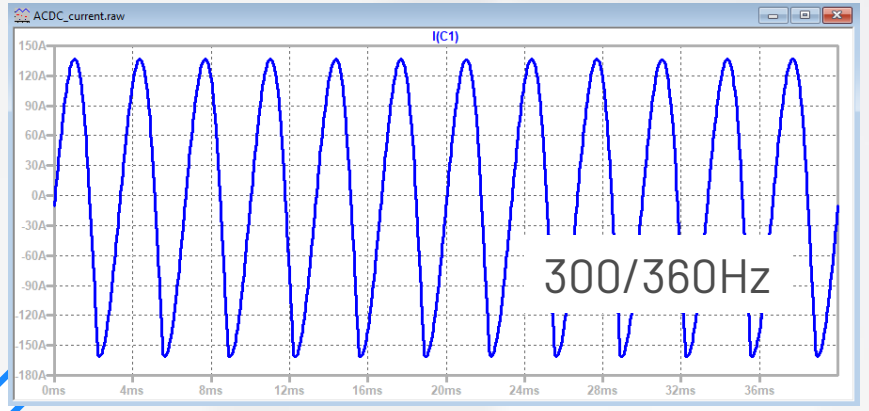
Comparisation of the parameters of the different aluminum electrolytic capacitors types

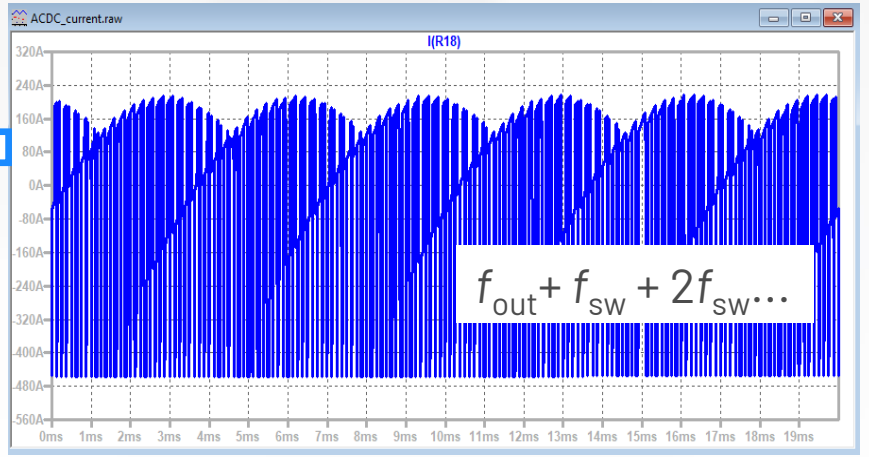
Electrolyte	Capacitance range	Rated voltage range	Typical ESR [1] 100 kHz, 20 °C	Typical ripple current [1] 100 kHz, 105 °C	Leakage current [1] after 2 minutes at 10 V
Non-solid borax or organic	0.1 µF–2.7 F	4–630 V	800 mΩ	130 mA	< 10 µA
Non-solid water-based	1–18000 µF	4–100 V	360 mΩ	240 mA	10 µA
Solid manganese dioxide	0.1–1500 µF	6.3–40 V[8]	400 mΩ	620 mA	12 µA
Solid conducting polymer	2.2–2700 µF	2–125 V[9]	25 mΩ	2.5 A	240 µA
Solid and non-solid hybrid electrolyte	6.8–1000 µF	6.3–125 V[10]	40 mΩ	1.5 A	100 µA

*source: https://en.wikipedia.org/wiki/Aluminum_electrolytic_capacitor

2. Problem description



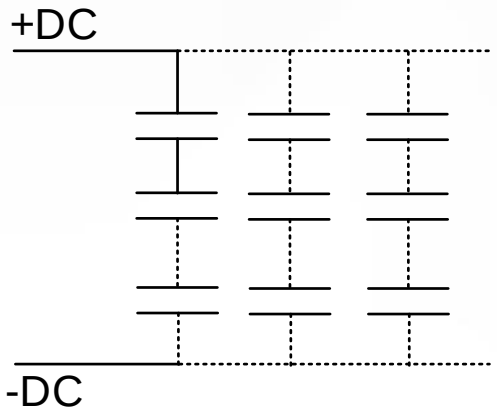




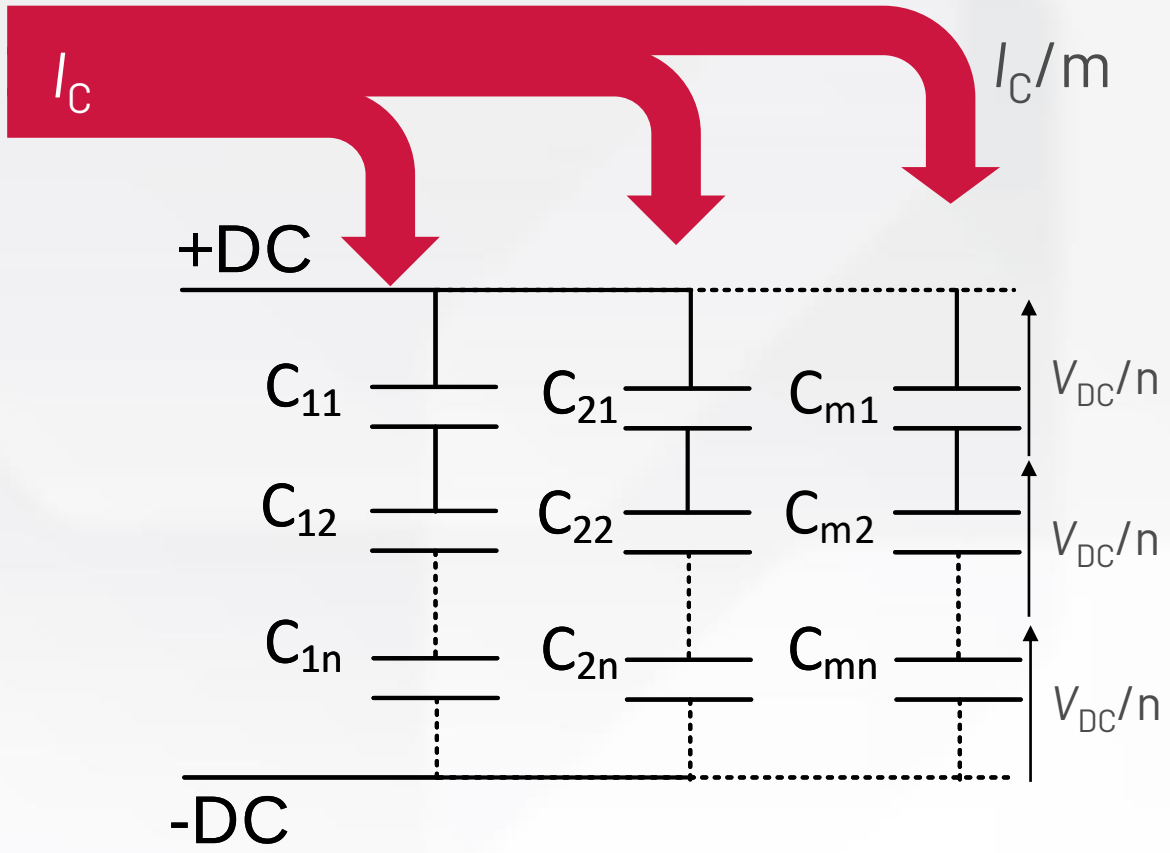
DC capacitor bank requirements

- Capacitance vs V_{DC} ripples
- High DC voltage operation
- **Handle LF and HF currents**

$I_C \sim 0.6\, I_{out}$



2. Problem description

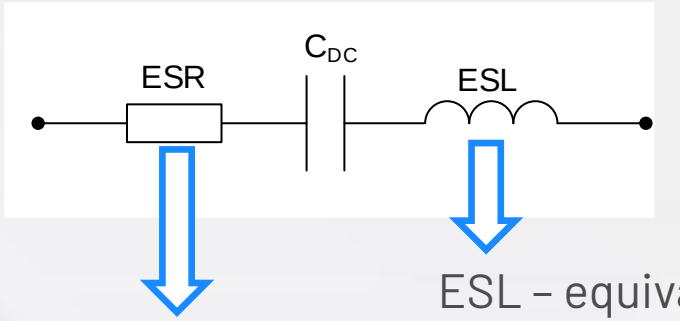


Series connection:
Voltage balancing required:
- easy to maintain (balancing resistors).

Parallel connection:
Current sharing/power losses:
- hard to predict and measure,
  - paracitic resistances & inductances,
  - capacitor parameters,
  - mechanical connections.

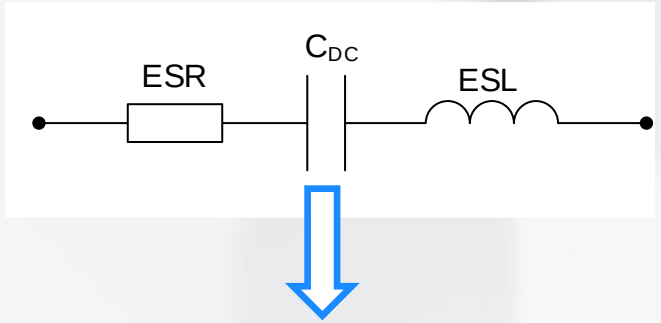
Setup with n=2 and m=4 was analyzed

3. Equivalent DC link capacitor model (ESR & ESL)

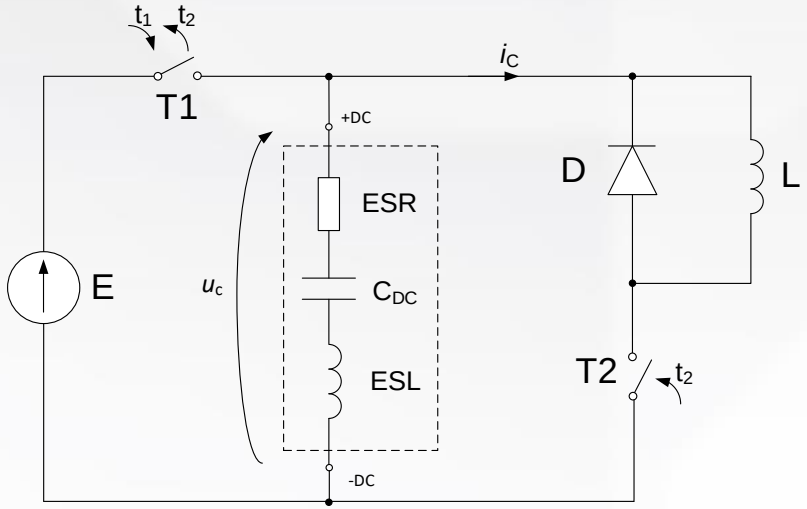


ESL – equivalent series inductance

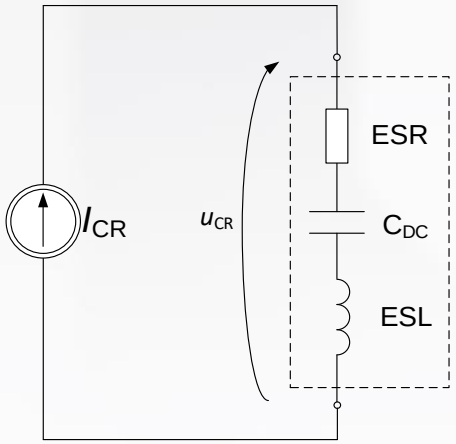
ESR – equivalent series resistance



C_{DC} – Capacitor capacitance

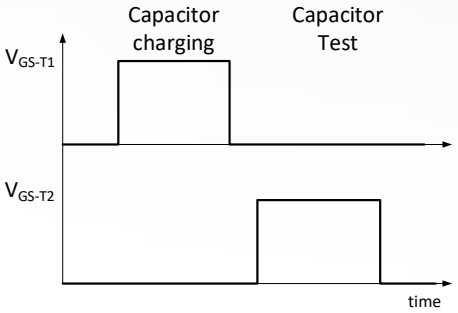


E & (I_{CR})



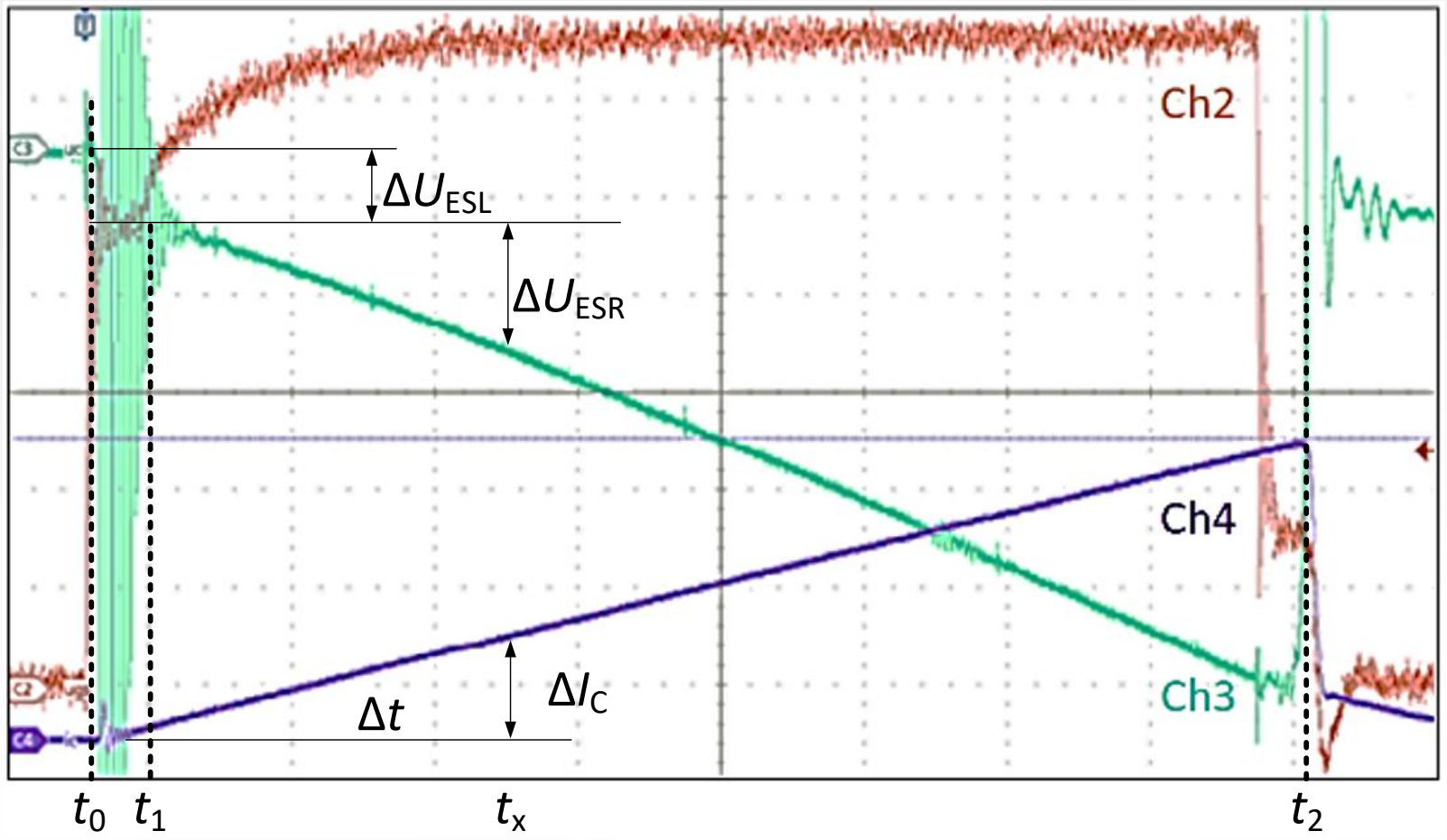
T1

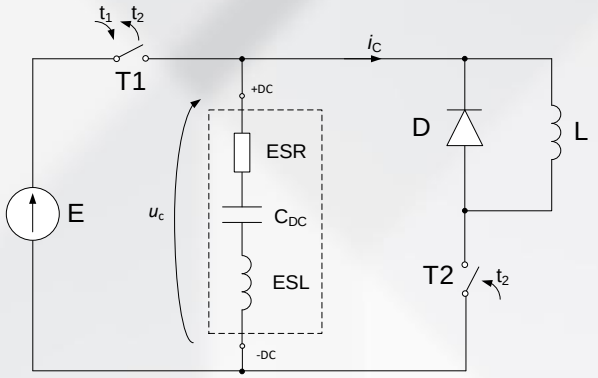
T2 + D



3. Equivalent DC link capacitor model (ESR & ESL)

Scope waveforms for ESR and ESL masurement of C_1





$\Delta U_{ESL} = 0.42\ V$
$\Delta I_C = 9.58\ A$
$\Delta t = 1.5\ us$

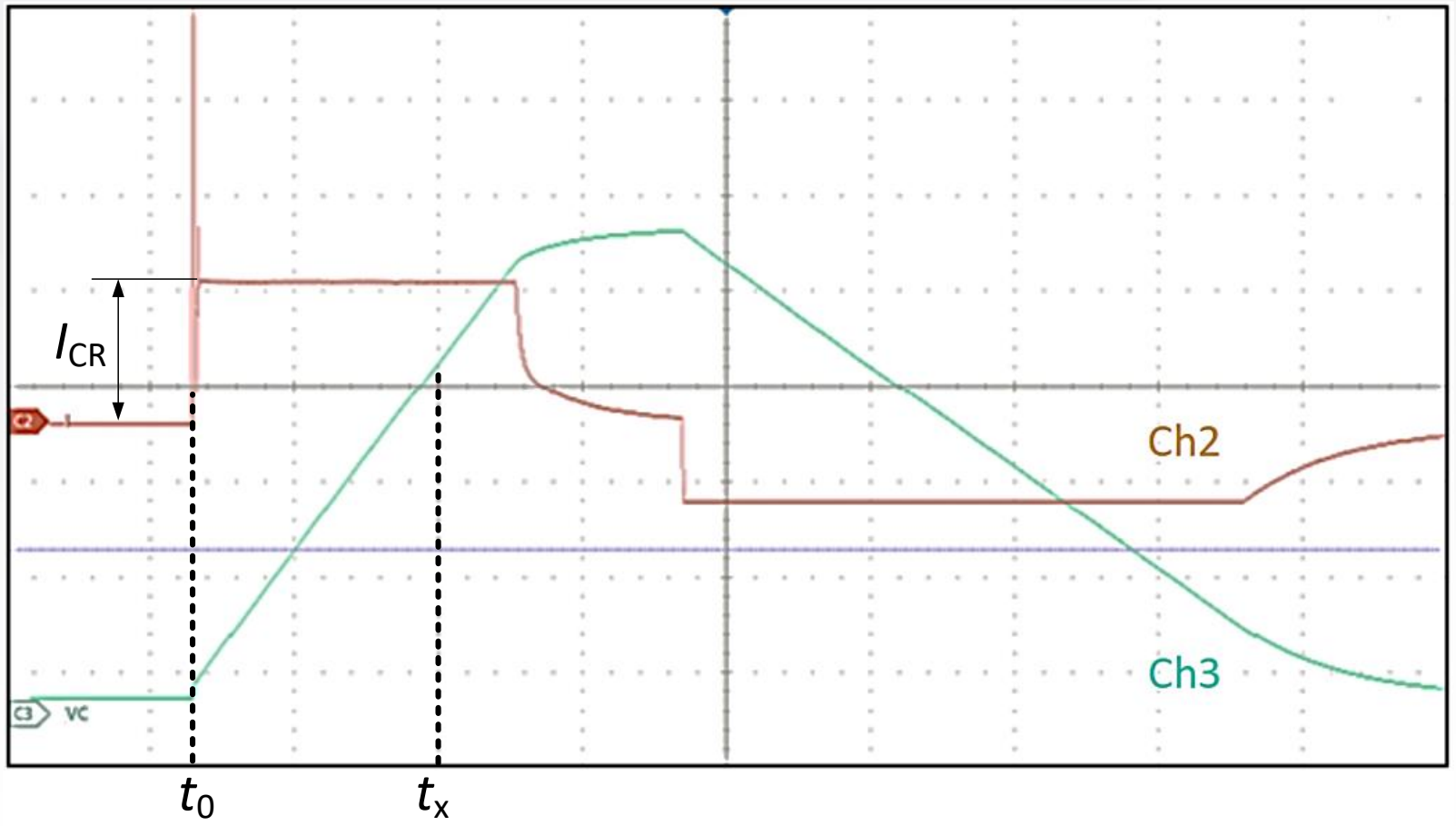
$$ESL = \frac{\Delta U_{ESL}}{\frac{\Delta I_C}{\Delta t}} = 65.77\ \text{nH}$$

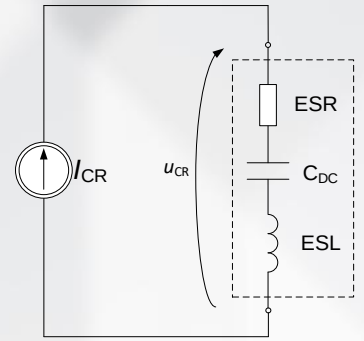
$\Delta U_{ESR} = 1.47\ V$
$I_C = 83.2\ A$

$$ESR = \frac{\Delta U_{ESR}}{I_c(t_x)} = 17.66\ \text{m}\Omega$$

3. Equivalent DC link capacitor model (C_{DC})

Scope waveforms for C_{DC} capacitance measurement of C_1





$I_{CR} = 148.4\,mA$
$\Delta t = 1.87s$
$\Delta U_{CE} = 74.26V$

$$C_{DC} = \frac{I_{CR}}{\frac{\Delta U_{CR}}{\Delta t}} = 3.74\,mF$$

3. Equivalent DC link capacitor model (C_{DC})

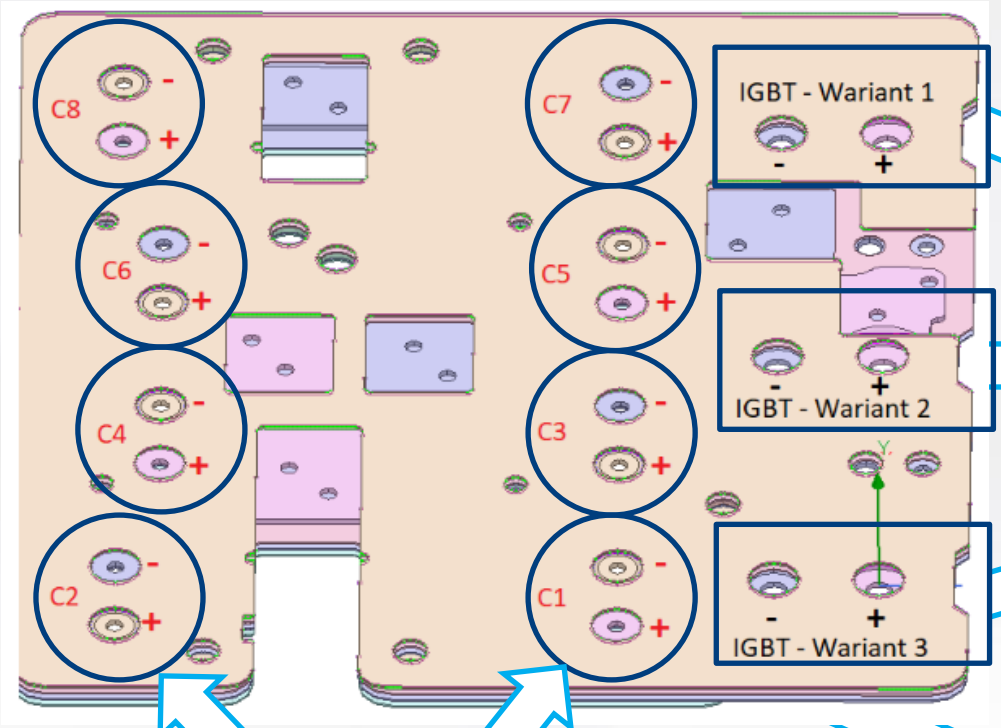
Test results for measured capacitors

	C [mF]	ESL [nH]	ESR [mΩ]
C1	3,74	65,77	17,66
C2	3,82	61,86	17,04
C3	3,90	55,56	17,35
C4	3,79	64,93	17,35
C5	3,91	57,02	16,72
C6	3,84	59,28	16,88
C7	3,98	56,99	16,72
C8	3,81	55,75	17,04

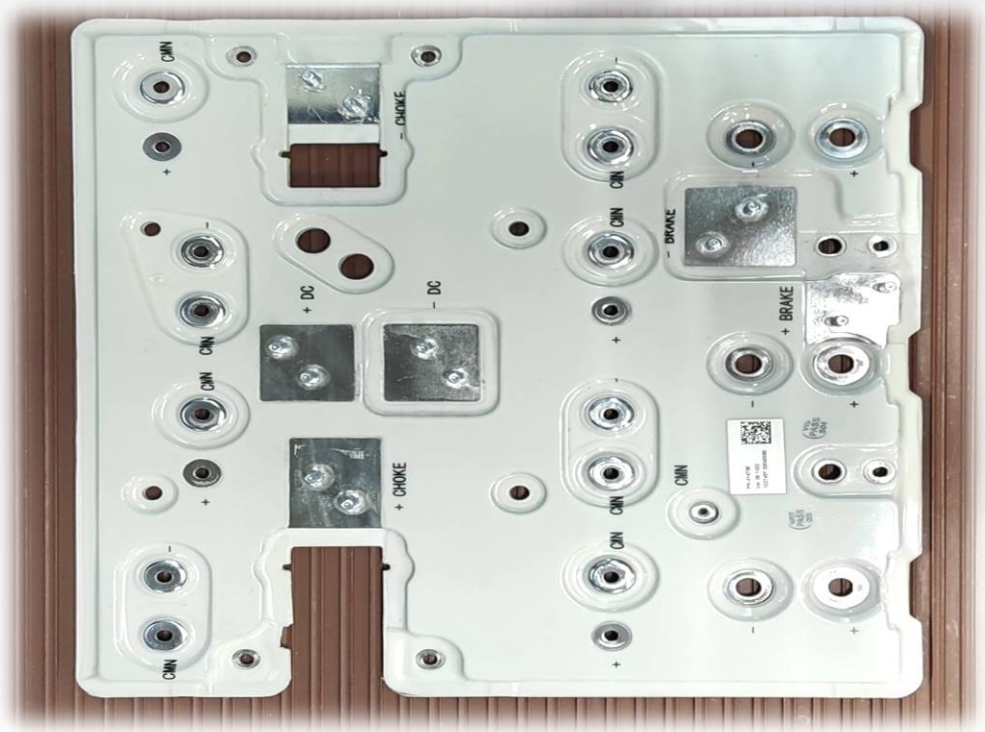
Datasheet

C = 4.1mF (+/-20%)
ESR_{max}= 20 mΩ
ESL_{max}= 50 nH

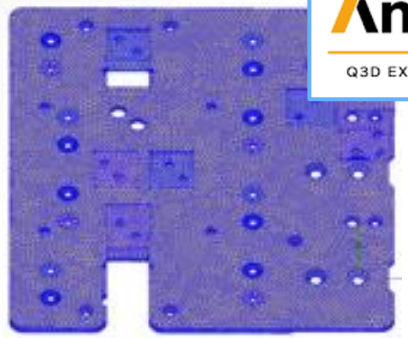
4. Laminated busbars ROM model



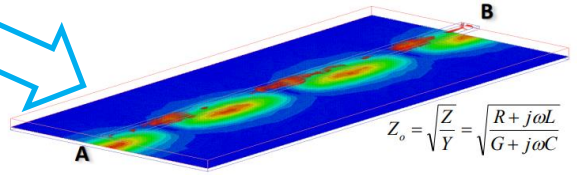
IGBT placement



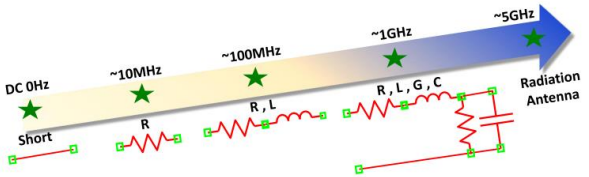
Capacitor placement



Ansys
Q3D EXTRACTOR

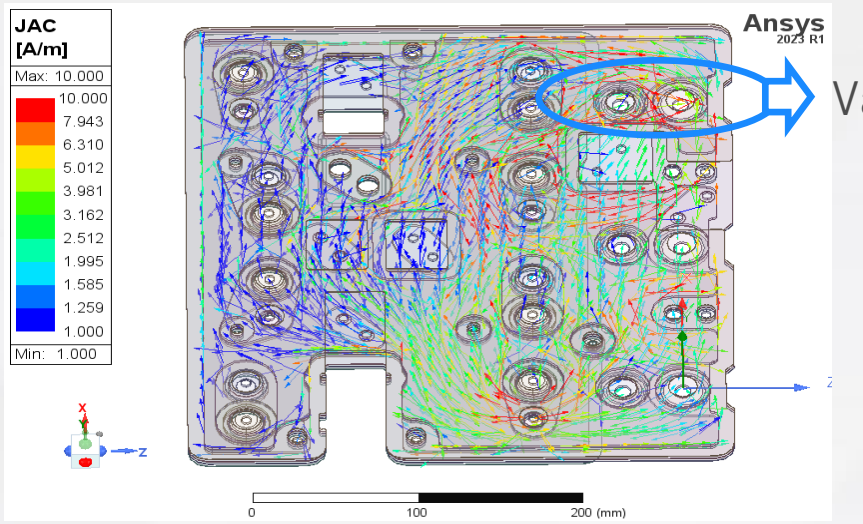


$$Z_o = \sqrt{\frac{Z}{Y}} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$$

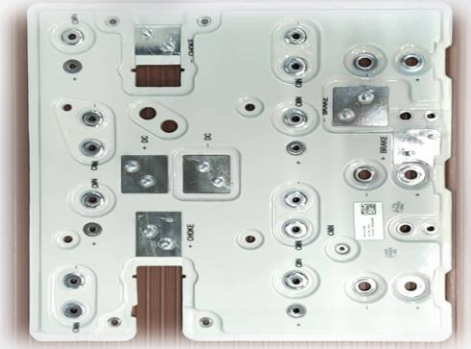


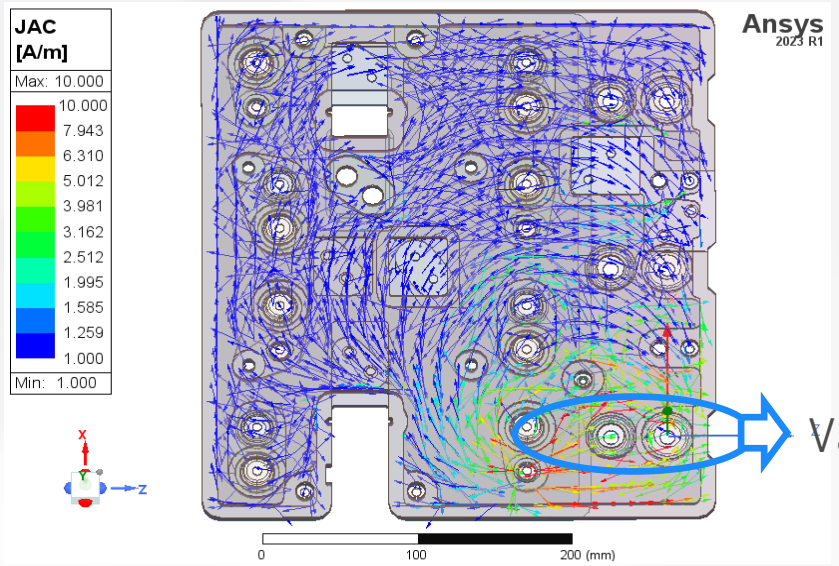
Rockwell Automation

4. Laminated busbars ROM model

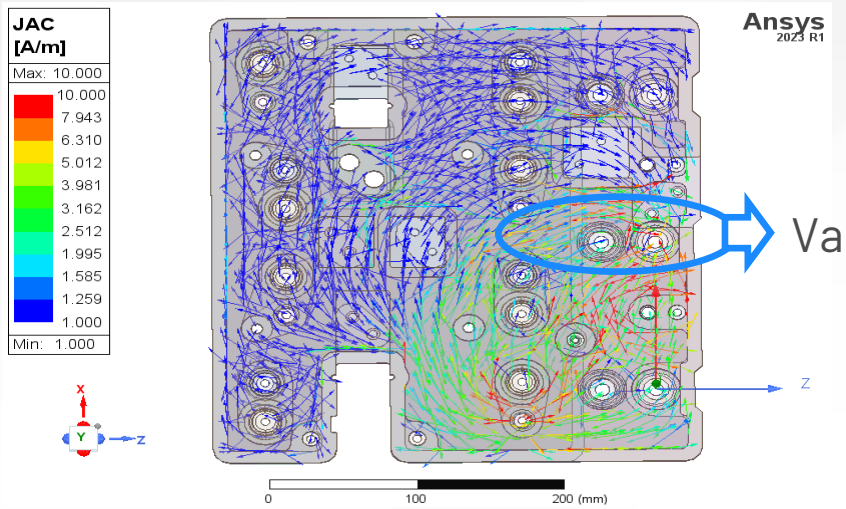


Variant 1





Variant 3



Variant 2

Big impact of laminated busbars design for current flow distribution

5. Multi-phisics simulations - model export

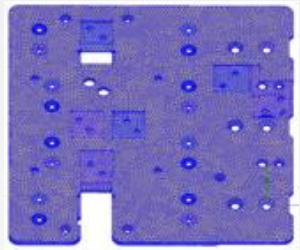
Ansys

MATLAB® & SIMULINK®

.cir file

ANSYS Q3D

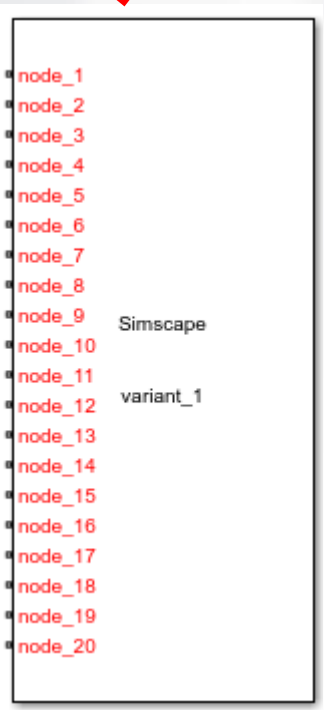
Extraction of RLCG parasitic parameters.



MATLAB Scripts

Generation Simscape model from CiR file

```
.subckt Variant_1_half 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18
+ 23 24 25 26 27 28 29 30 31 32 33 34
V1 1 35 dc 0.0
V2 2 36 dc 0.0
V3 3 37 dc 0.0
V4 4 38 dc 0.0
V5 5 39 dc 0.0
V6 6 40 dc 0.0
V7 7 41 dc 0.0
V8 8 42 dc 0.0
V9 9 43 dc 0.0
V10 10 44 dc 0.0
V11 11 45 dc 0.0
V12 12 46 dc 0.0
V13 13 47 dc 0.0
V14 14 48 dc 0.0
V15 15 49 dc 0.0
V16 16 50 dc 0.0
V17 17 51 dc 0.0
R1 35 52 2.54973164823e-05
R2 36 53 4.30041411191e-05
R3 37 54 1.93964491272e-05
R4 38 55 2.39165563367e-05
R5 39 56 2.24001356977e-06
R6 40 57 2.56144775532e-05
R7 41 58 8.29661459903e-06
R8 42 59 3.29168773971e-05
R9 43 60 4.58835254491e-05
R10 44 61 1.95571916746e-05
R11 45 62 2.88773239354e-05
R12 46 63 1.04887419661e-05
R13 47 64 8.31371029309e-05
R14 48 65 7.88022466381e-05
R15 49 66 6.43035043551e-05
R16 50 67 9.40803089212e-05
R17 51 68 1.27501083746e-06
F1_2 52 35 V2 0.508074
F1_3 52 35 V3 0.659486
F1_4 52 35 V4 0.452973
F1_5 52 35 V5 -0.00631487
F1_6 52 35 V6 0.407966
F1_7 52 35 V7 0.0778246
F1_8 52 35 V8 0.312353
F1_9 52 35 V9 0.0477824
F1_10 52 35 V10 0.0821684
```

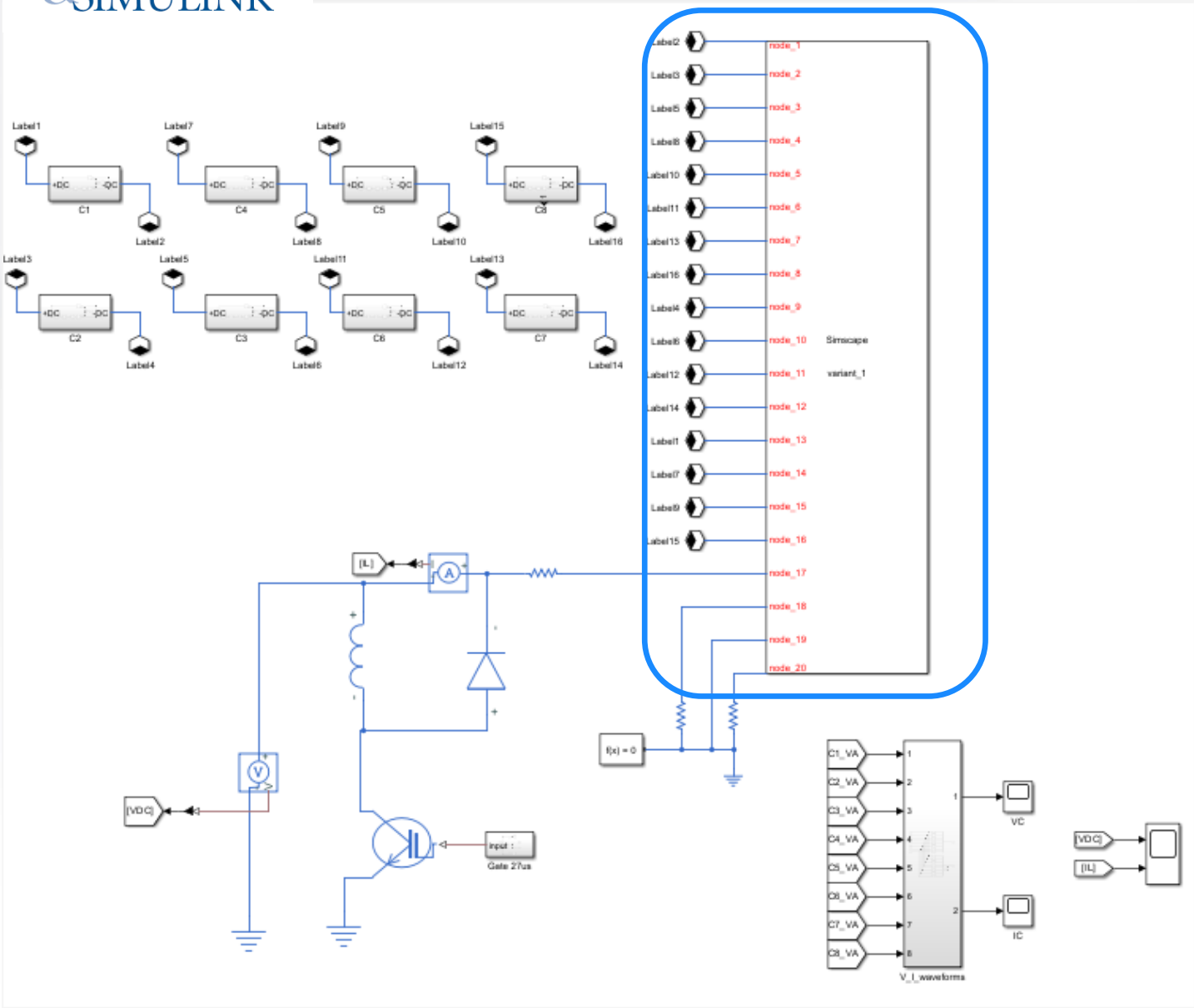


Oprogramowanie Naukowo-Techniczne sp. z o.o.

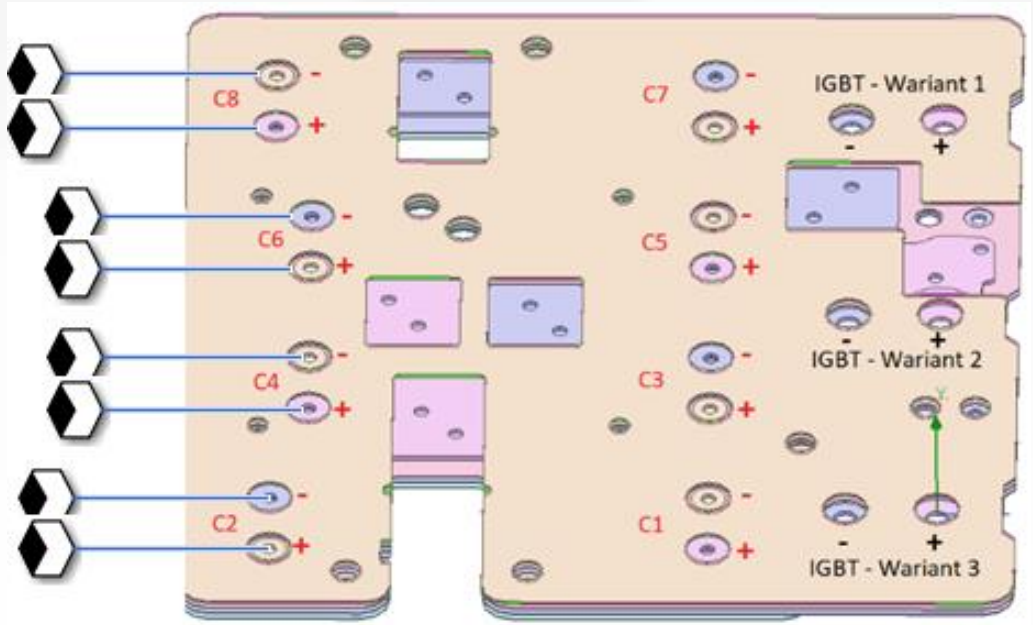
Gernot Schraberger

Rockwell Automation

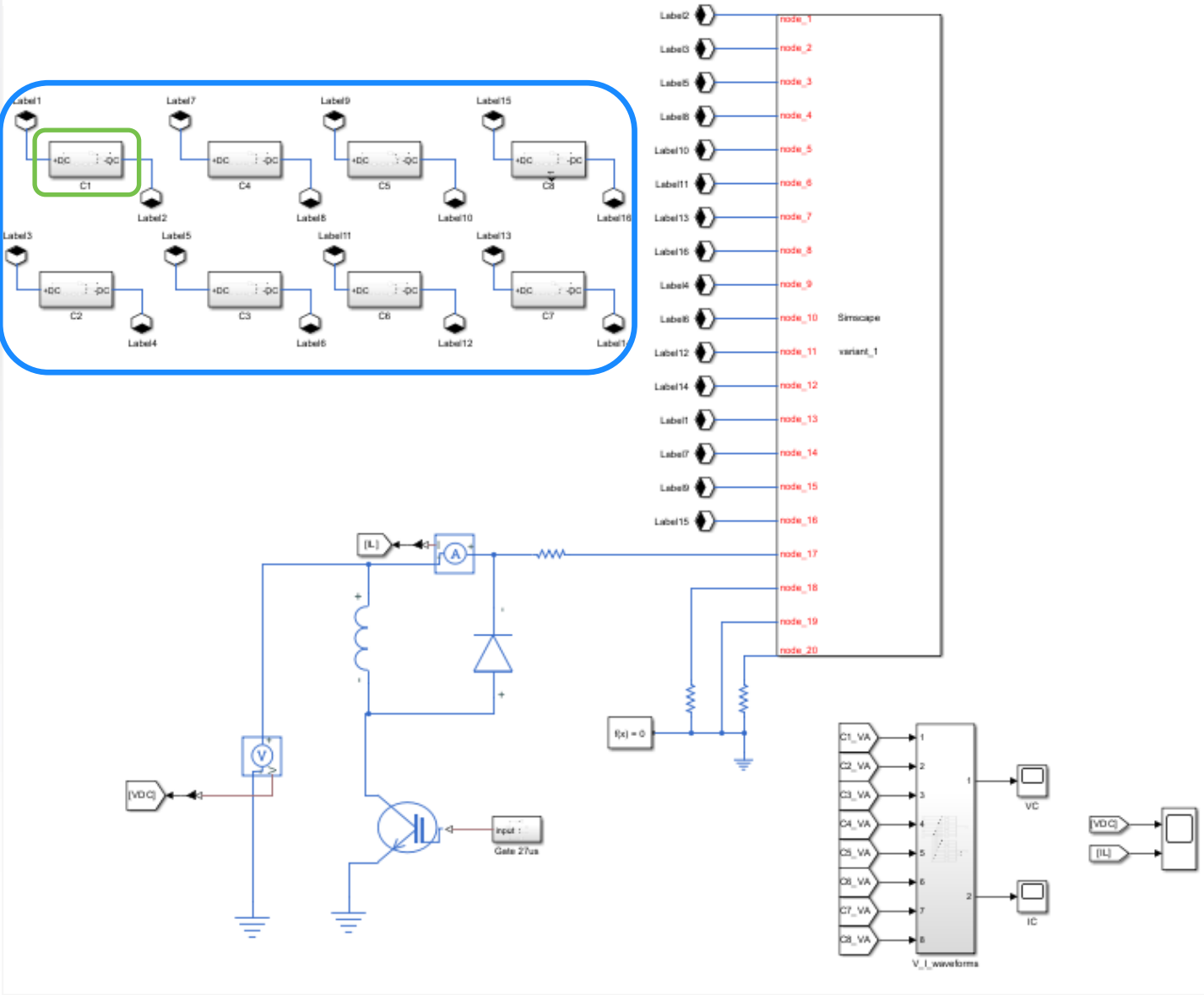
5. Multi-phisics circuit simulations – pulse test



1. Busbars Q3D model (ROM model)
2. Capacitors RLC models
3. IGBT + Inductor

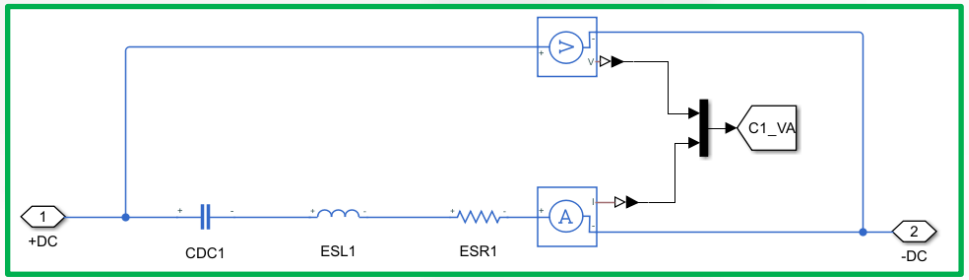


5. Multi-phisics circuit simulations – pulse test



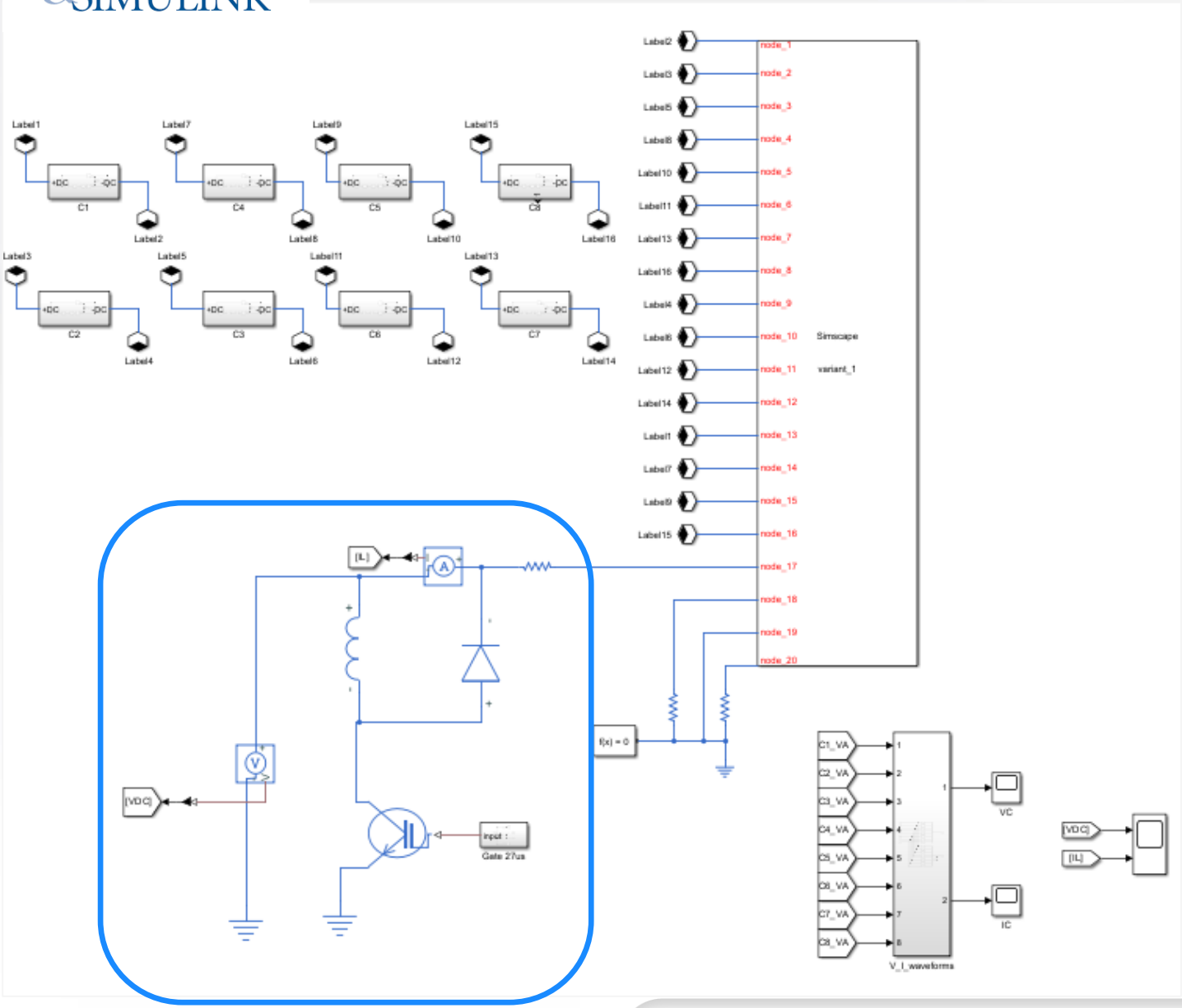
1. Busbars Q3D model (ROM model)
2. Capacitors RLC models
3. IGBT + Inductor

Single capacitor model



8 capacitors
575 V/4.1 mF

5. Multi-phisics circuit simulations – pulse test

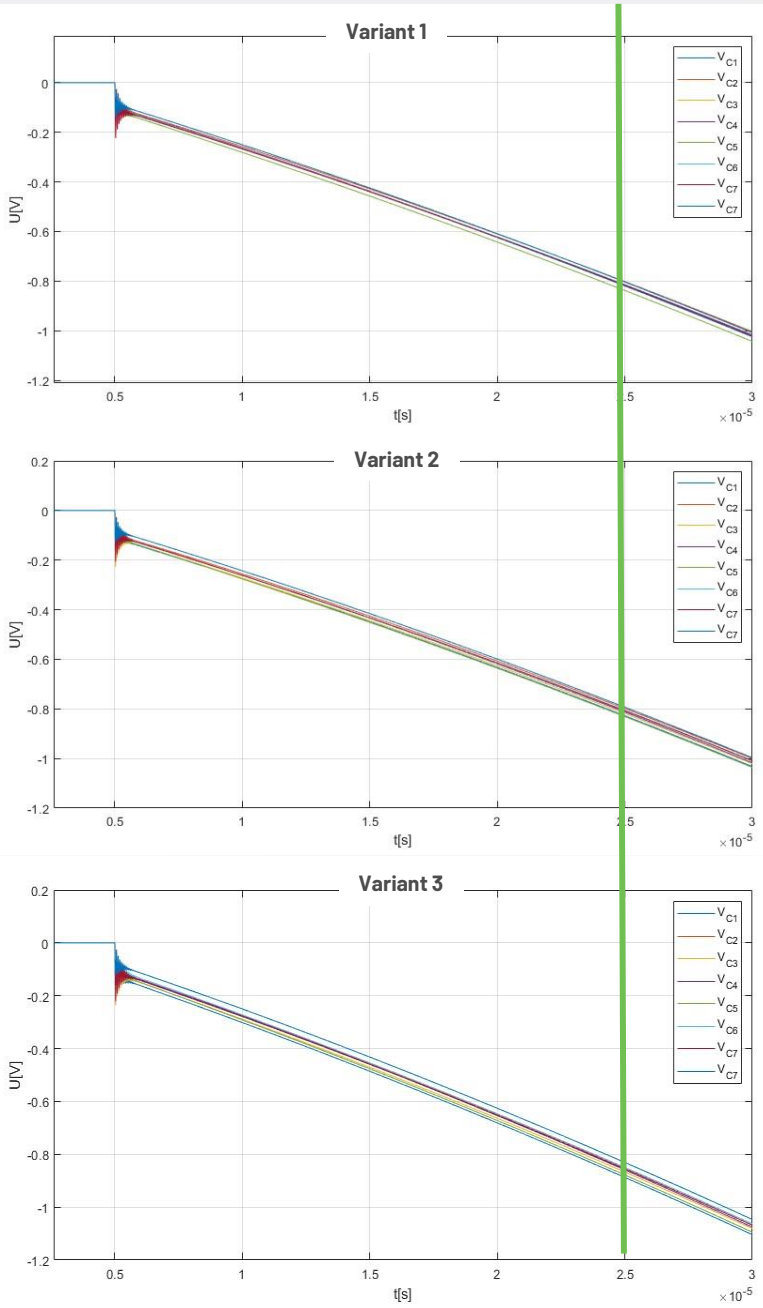


1. Busbars Q3D model (ROM model)
2. Capacitors RLC models
3. IGBT + Inductor

1.2kV/1.2kA

25mm^2
~6 turns
d ~35-50cm

5. Multi-phisics circuit simulations



	Variant 1	Variant 2	Variant 3
U_{C1} [mV]	764	797	810
U_{C2} [mV]	752	774	783
U_{C3} [mV]	761	788	791
U_{C4} [mV]	763	787	793
U_{C5} [mV]	777	796	800
U_{C6} [mV]	759	781	787
U_{C7} [mV]	759	770	790
U_{C8} [mV]	755	772	780

	C [mF]	ESL [nH]	ESR [mΩ]
C1	3,74	65,77	17,66
C2	3,82	61,86	17,04
C3	3,90	55,56	17,35
C4	3,79	64,93	17,35
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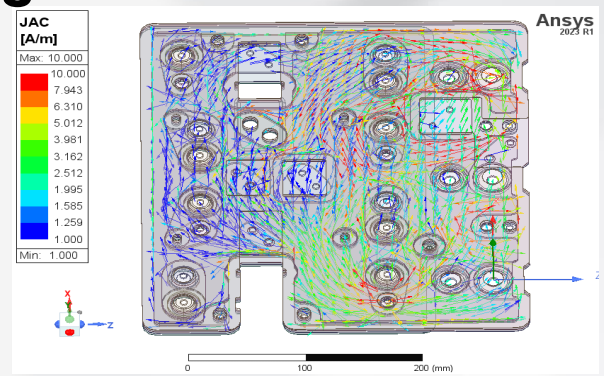
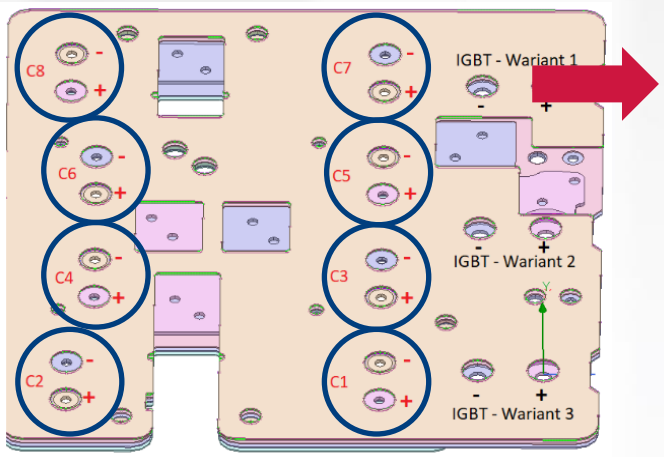
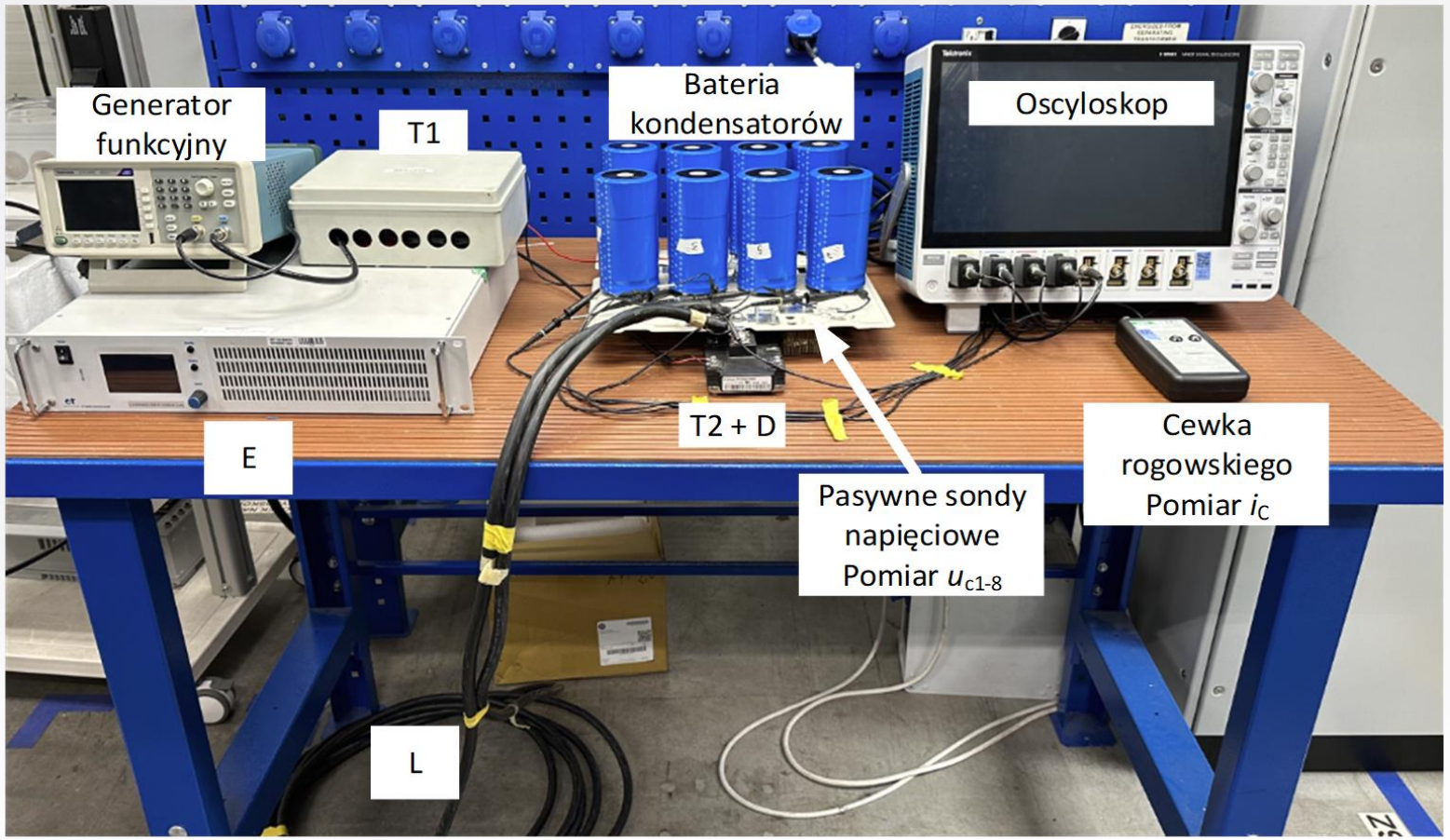
C8	3,81	55,75	17,04

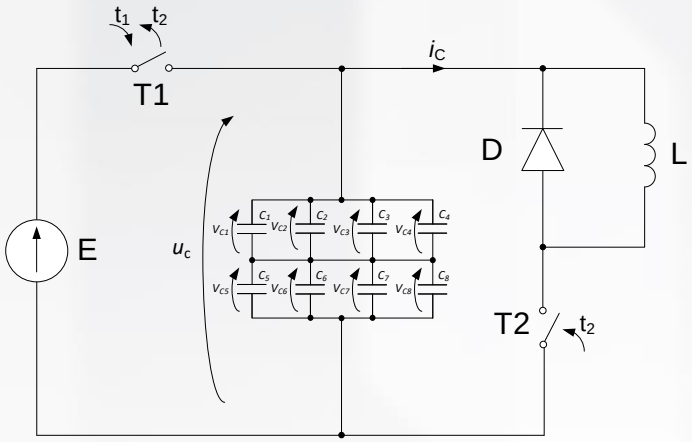




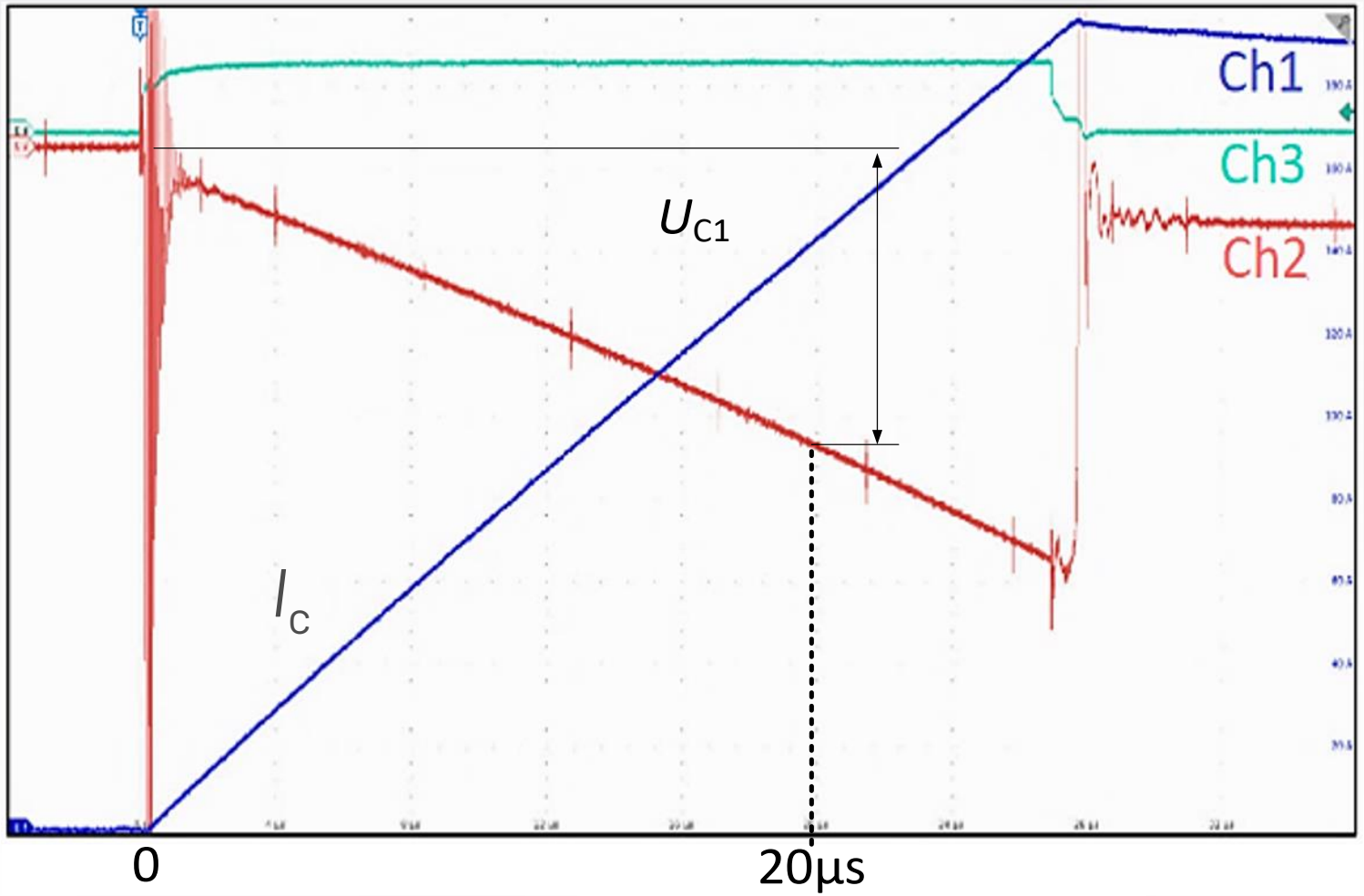
Rockwell Automation

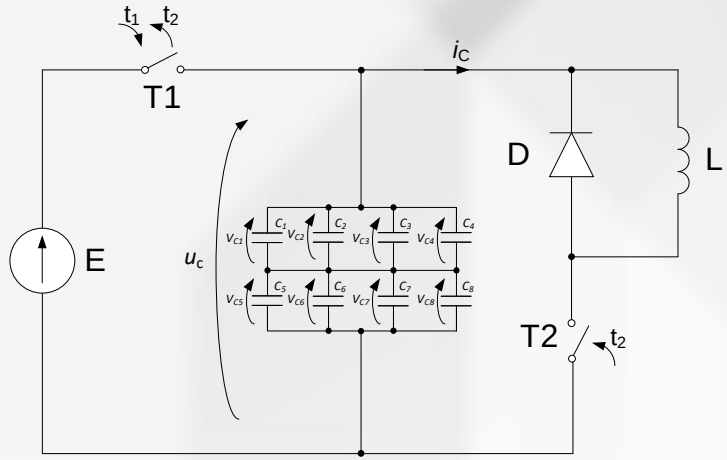
6. ROM Model validation – test setup





6. ROM Model validation – test results

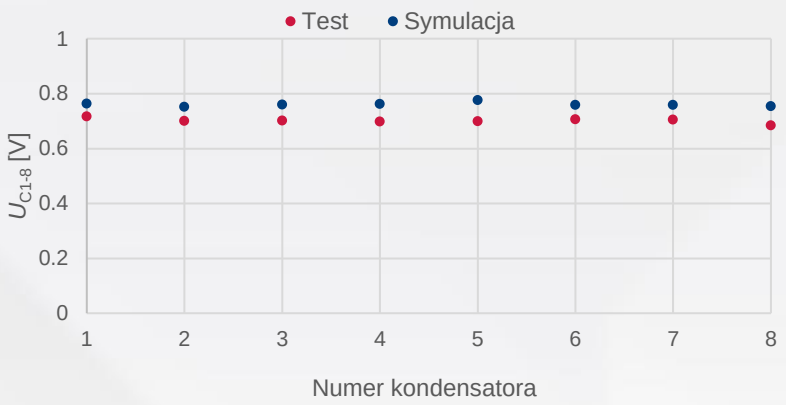




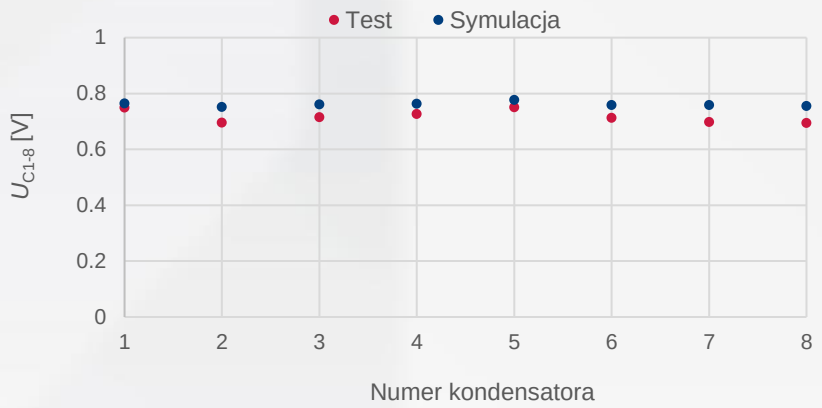
	Variant 1	Variant 2	Variant 3
U_{C1} [V]	0,717	0,750	0,758
U_{C2} [V]	0,701	0,696	0,715
U_{C3} [V]	0,702	0,715	0,730
U_{C4} [V]	0,699	0,727	0,728
U_{C5} [V]	0,700	0,751	0,748
U_{C6} [V]	0,707	0,713	0,709
U_{C7} [V]	0,706	0,698	0,712
U_{C8} [V]	0,685	0,695	0,705

6. ROM Model validation - summary

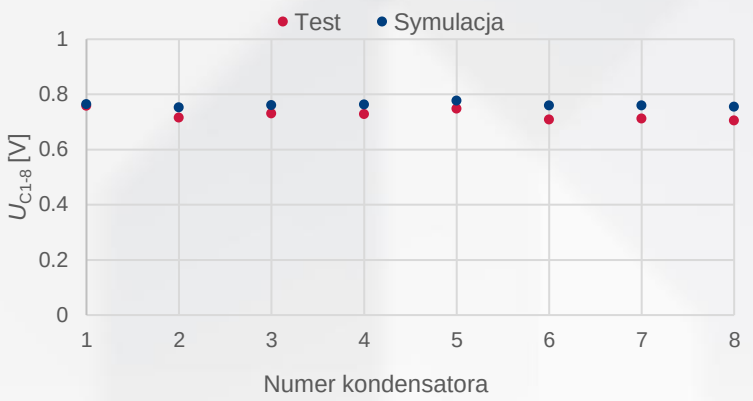
Variant 1



Variant 2

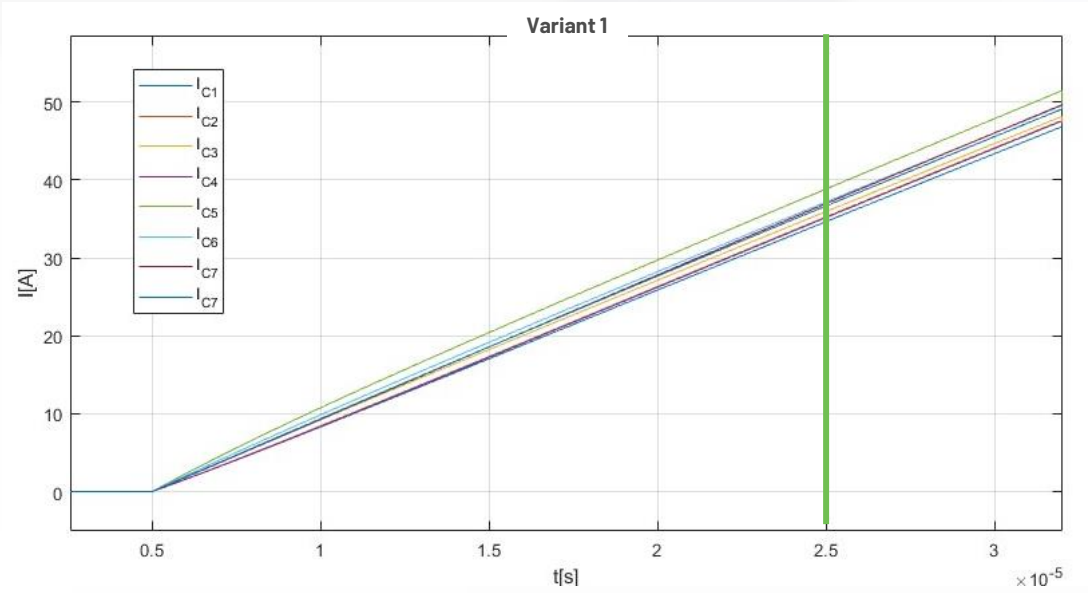


Variant 3



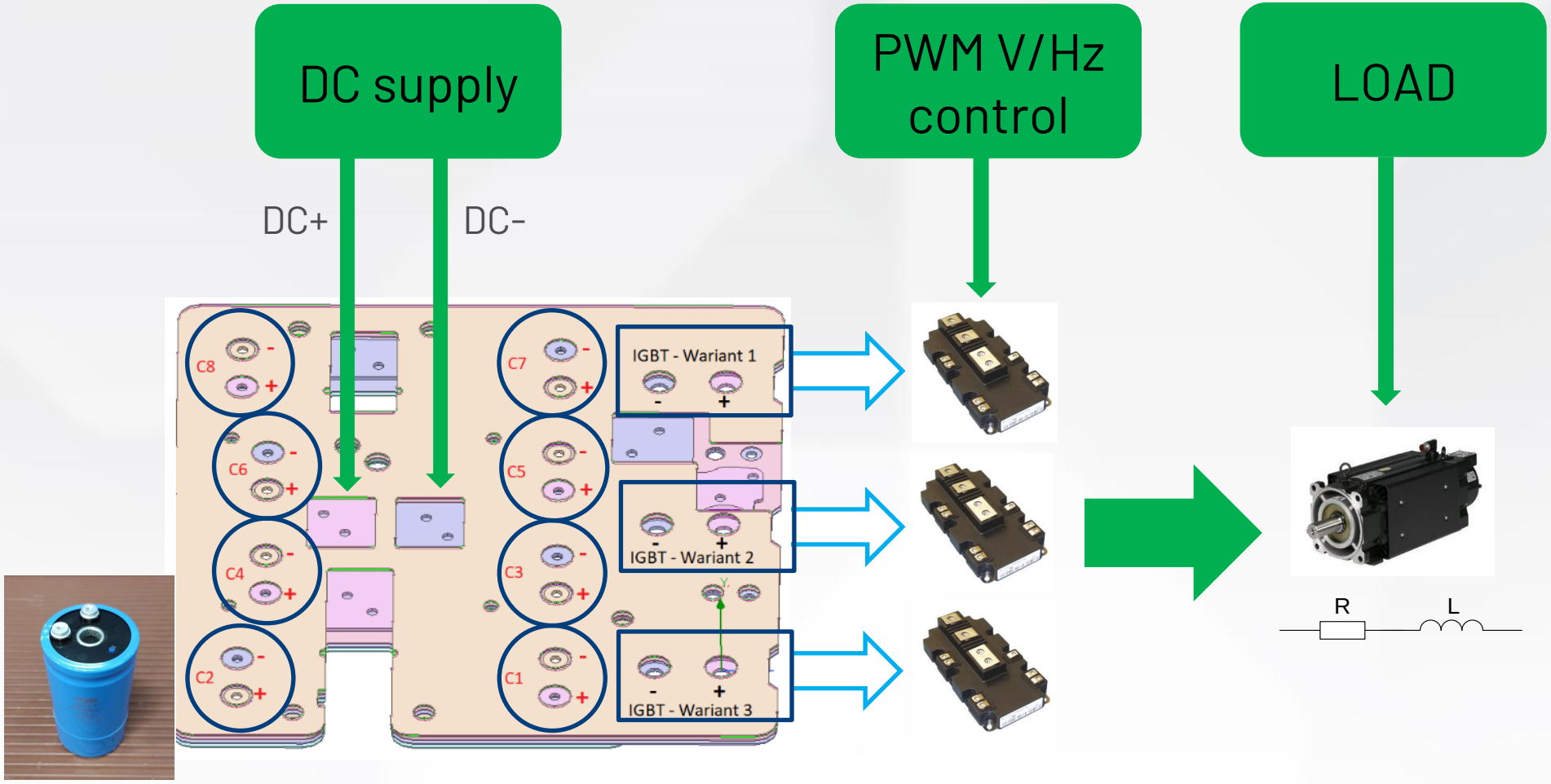
	Variant 1	Variant 2	Variant 3
I_{C1} [A]	32,45	33,65	34,44
I_{C2} [A]	33,14	33,93	34,54
I_{C3} [A]	33,68	34,69	35,00
I_{C4} [A]	32,96	33,75	34,23
I_{C5} [A]	36,11	36,77	37,19
I_{C6} [A]	34,76	35,53	36,09
I_{C7} [A]	34,52	35,24	35,93
I_{C8} [A]	34,57	35,23	35,70

11% higher current for C_5 in compare to C_1

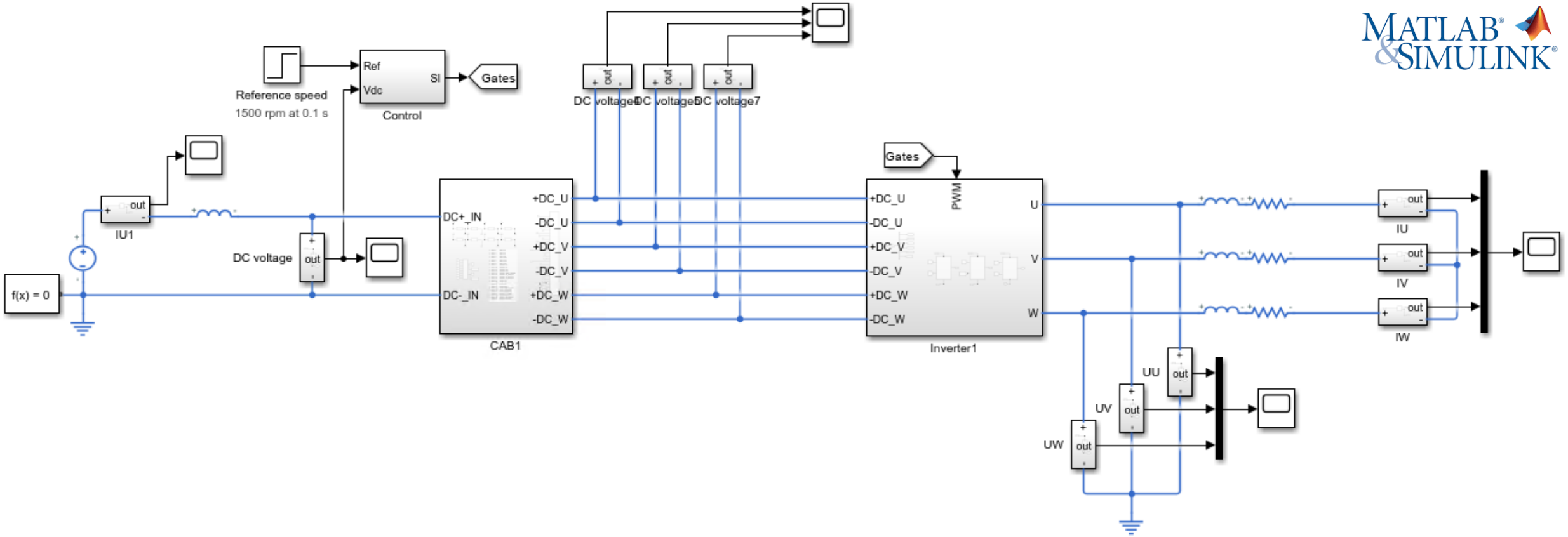


20us

7. DC/AC inverter simulations with busbar ROM model

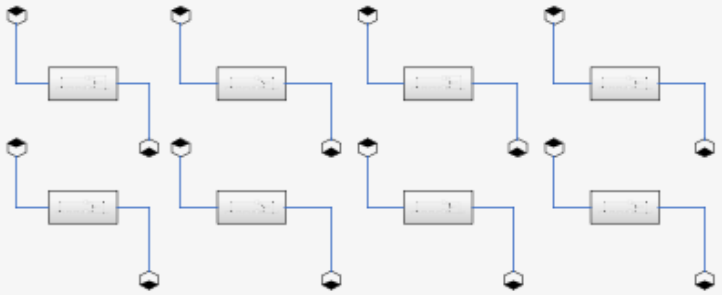


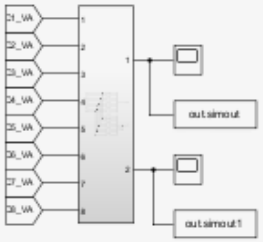
7. DC/AC inverter simulations with busbar ROM model – Simscape model

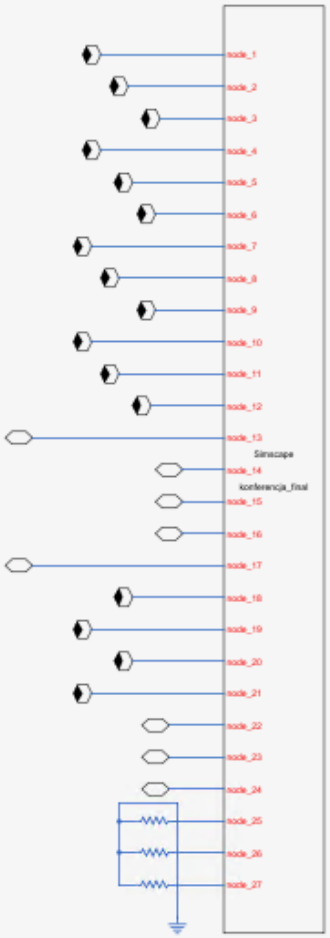


7. DC/AC inverter simulations with busbar ROM model – Simscape model

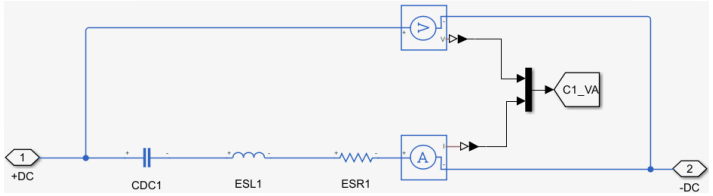
CAB1



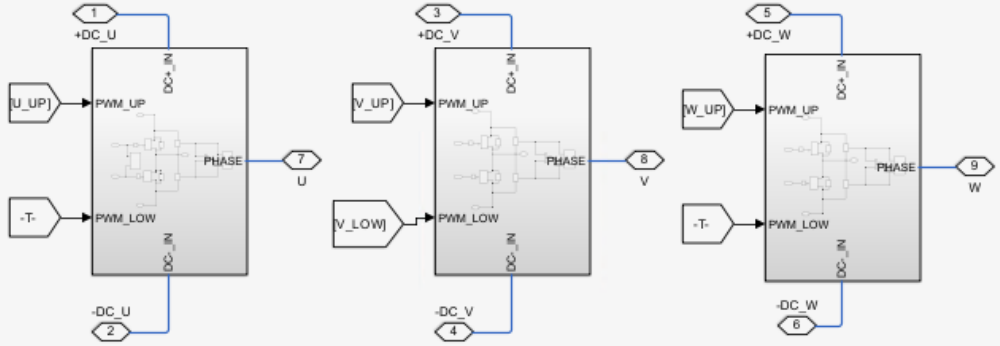


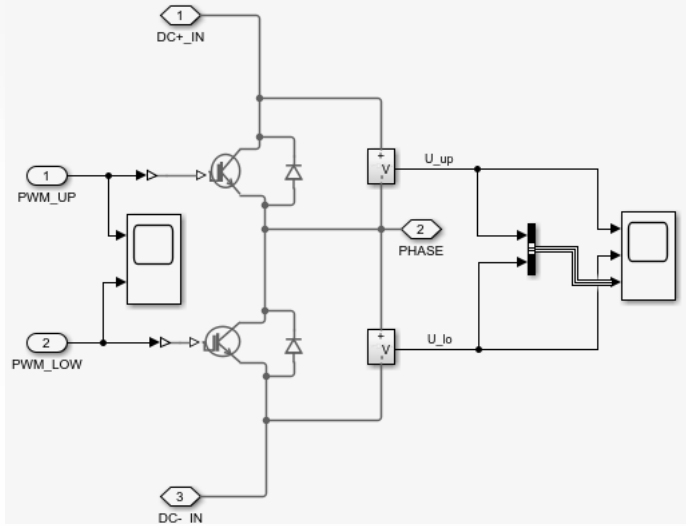



```
* node 1    MID:C2
* node 2    MID:C3
* node 3    MID:C5
* node 4    MID:C8
* node 5    MID:C10
* node 6    MID:C11
* node 7    MID:C13
* node 8    MID:C16
* node 9    MINUS:C4
* node 10   MINUS:C6
* node 11   MINUS:C12
* node 12   MINUS:C14
* node 13   MINUS:INPUT_MINUS
* node 14   MINUS:T1_Output
* node 15   MINUS:T2_Output
* node 16   MINUS:T3_Output
* node 17   PLUS:C1
* node 18   PLUS:C7
* node 19   PLUS:C9
* node 20   PLUS:C15
* node 21   PLUS:INPUT_PLUS
* node 22   PLUS:T1_Input
* node 23   PLUS:T2_Input
* node 24   PLUS:T3_Input
* node 25   MID:SinkMid
* node 26   MINUS:SinkMinus
* node 27   PLUS:SinkPlus
```

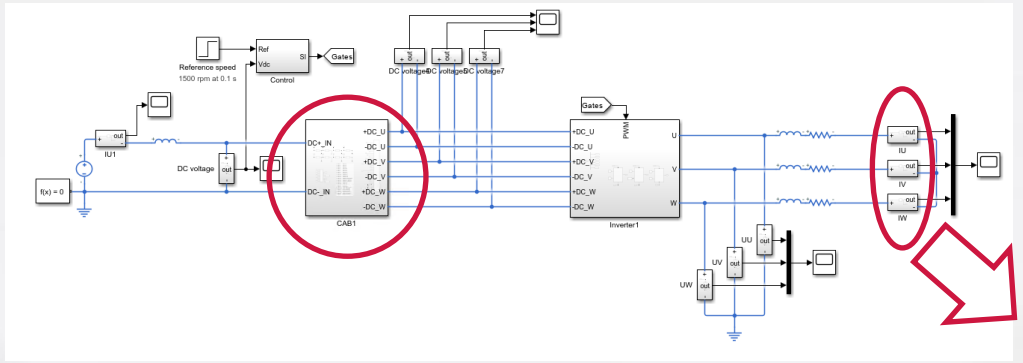


INVERTER1



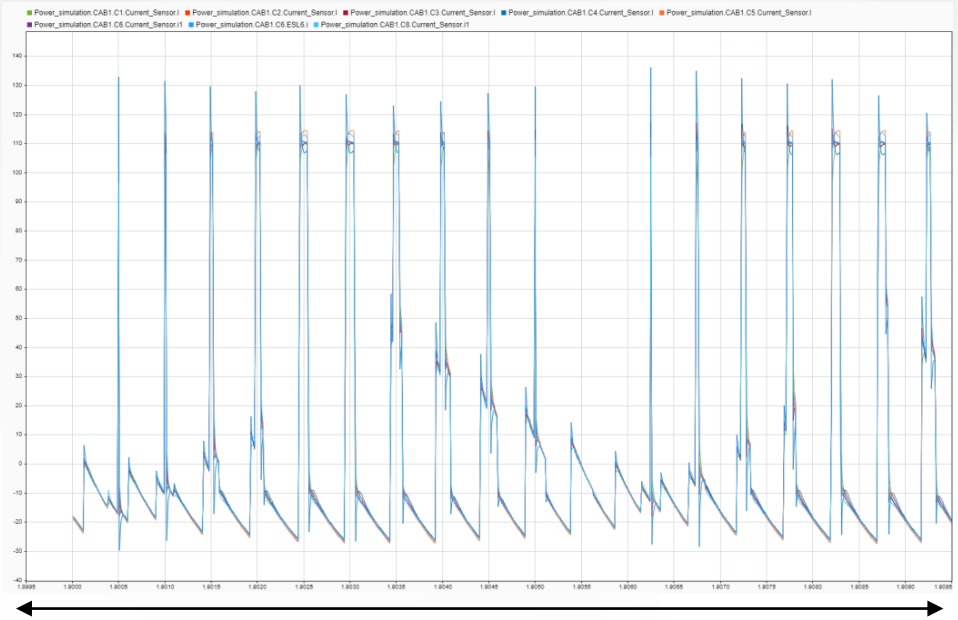


7. DC/AC inverter simulations with busbar ROM model – simulation results



Steady state, 1.9s to 2.0s
2h25m of simulation

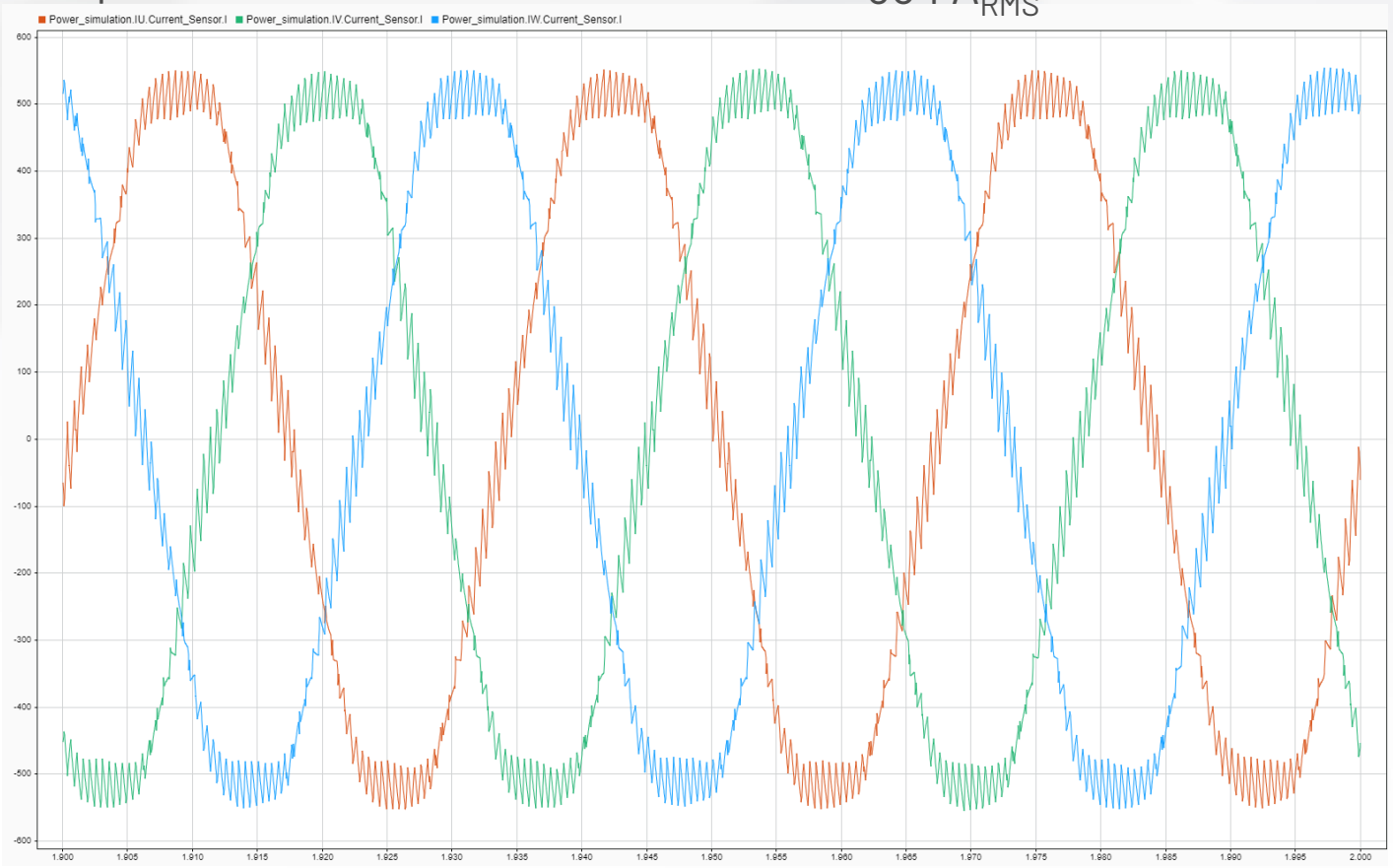
Capacitors currents



10ms

Output currents

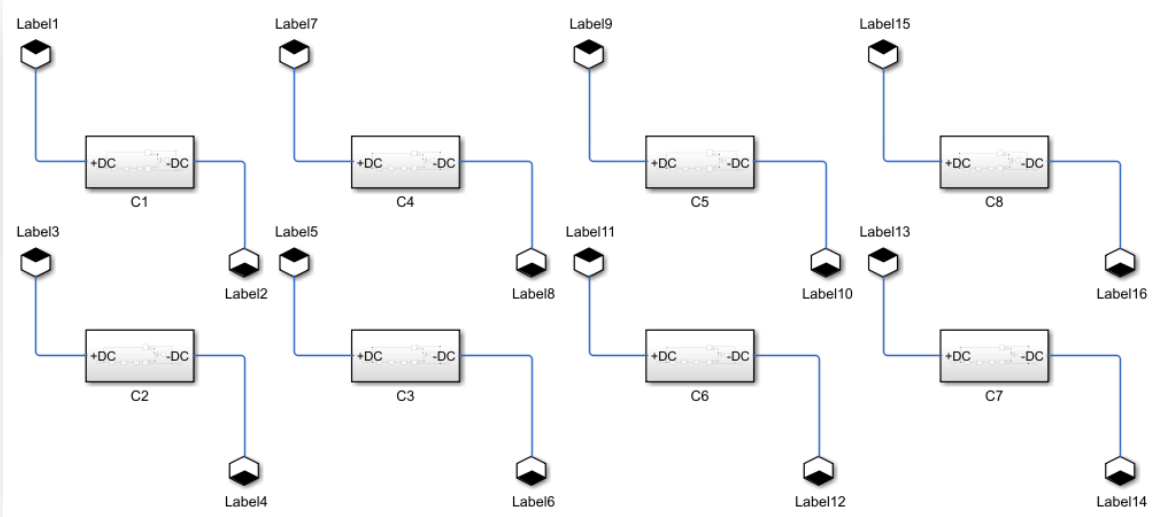
~354 A_{RMS}

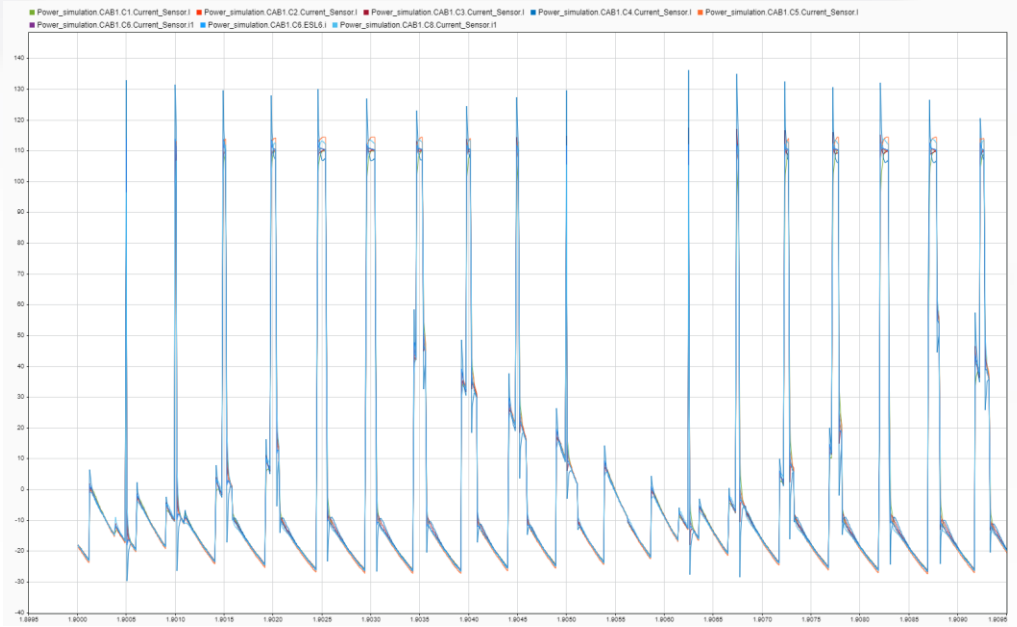


100ms

7. DC/AC inverter simulations with busbar ROM model – simulation results

Capacitors current	
I_{C1} [A]	35,3
I_{C2} [A]	35,9
I_{C3} [A]	36,1
I_{C4} [A]	36,8
I_{C5} [A]	37,2
I_{C6} [A]	36,4
I_{C7} [A]	37,1
I_{C8} [A]	36,3





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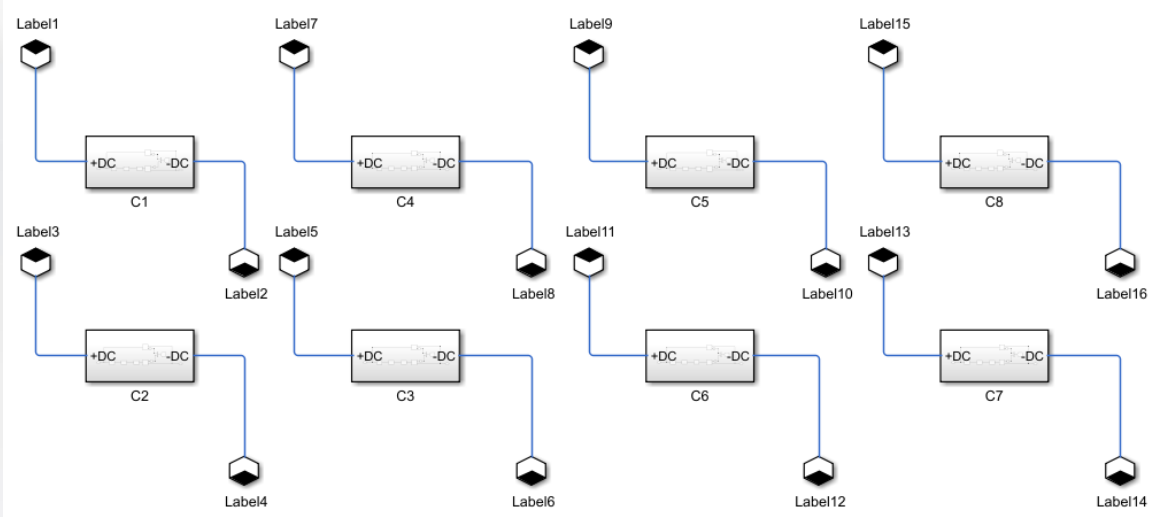
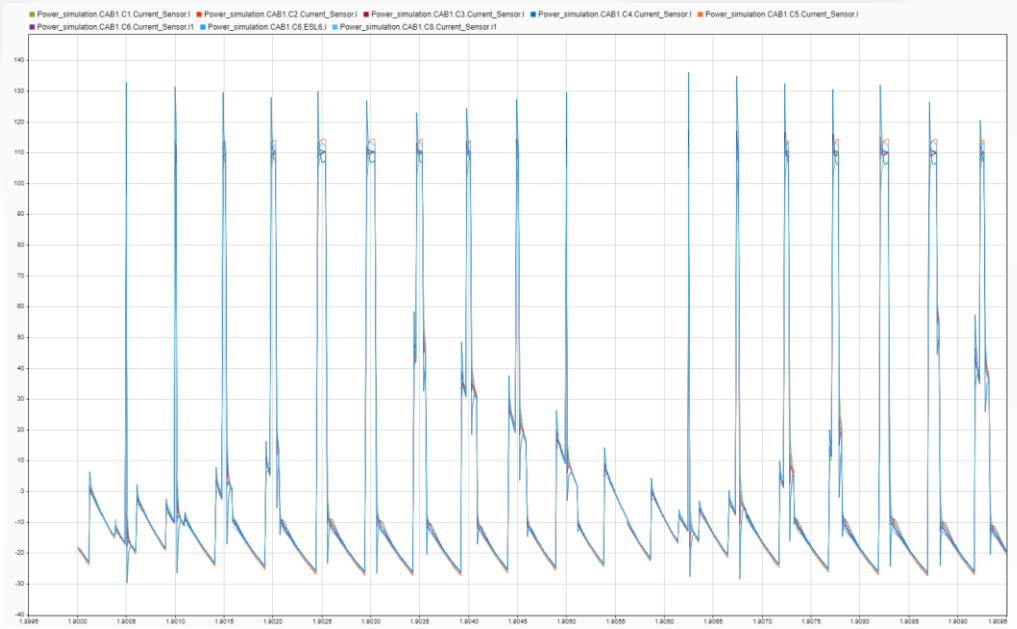
I_{C4} [A]	36,8
I_{C5} [A]	37,2
I_{C6} [A]	36,4
I_{C7} [A]	37,1
I_{C8} [A]	36,3





	Variant 1	Variant 2	Variant 3	Mean
I_{C1} [A]	32,45	33,65	34,44	33.5
I_{C2} [A]	33,14	33,93	34,54	33.9
I_{C3} [A]	33,68	34,69	35,00	34.5
I_{C4} [A]	32,96	33,75	34,23	33.6
I_{C5} [A]	36,11	36,77	37,19	36.7
I_{C6} [A]	34,76	35,53	36,09	35.5
I_{C7} [A]	34,52	35,24	35,93	35.2
I_{C8} [A]	34,57	35,23	35,70	35.2

Slaid 22

8. Summary & future research

Presented methodology demonstrates significant potential to be used during capacitor bank design or optimization for extended product lifetime

- Busbar layout has big impact on current sharing
- Detailed capacitors parameters should be considered
- Possibility to determine currents flowing through each capacitor

Methodology improvement needed:

- Temperature impact on current sharing
- Comparison of different available measurement method for capacitor parameters

Simulation tools

- MATLAB/Simulink environment allows for simple and transparent way of importing .cir model from Ansys environement,
- Busbar ROM models can be used to build more advanced multiphisics simulation models
- Model optimization required to speed-up simulation time

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